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on

Advanced Communication Systems & Applications

25th & 26th June 2013

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PREFACE

Dear Distinguished Delegates and Guests,

It is my pleasure to welcome everybody at MITS for the National Conference on Advanced Communication Systems & Applications, held on June 25th & 26th 2013 organized by the Department of Electronics & Communication Engineering, MITS, Madanapalle with the support of TEQIP-II. The main goal of the conference is to provide scientific forums for sharing of knowledge through discussions in Nationwide.

Now a days the research is on multi-disciplines rather than on single area. This National Conference provides a common platform for all the academicians, researchers and executives from industry to share their innovative ideas in multi-disciplines at a time. This conference provides opportunity for academic staff, research scholars and industrialists to present their research works and is a stage for exchange of new ideas in the fields of Science & Technology.

We have invited research papers from various streams like Communication systems, Embedded & VLSI Technology, Signal Processing, Robotics & Automation, Security Protocols and Encryption systems, Wi-Max, Wi-Fi, Bluetooth & Zig Bee, Mobile cellular system, Smart Antennas and Satellite Communications. I am very glad to observe that the response is tremendous from various individuals from different places. Our technical team has been selected 41 quality papers after pear review and plagiarism check for the presentation in the National Conference-Advanced Communication Systems & Applications. I congratulate the selected participants, for their contribution to present their research papers at this knowledge hub.

I am very much thankful to the management for their continuous encouragement and support in organization of such events. I am expressing my heartfelt thanks to the Principal, TEQIP-II Coordinator, Head of the Dept. ECE and my colleagues who contributed their support in organization of this National Conference with a grand success.

With best regards

Dr. D. Asha devi

Program coordinator

MESSAGE

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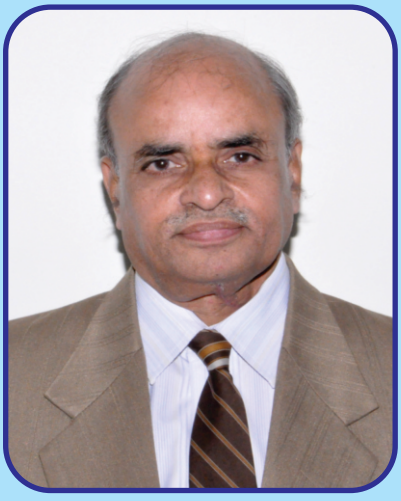

Globalization of technical education and technology development is forcing the engineers, academicians and research scholars to concentrate on latest trends in technology and update their knowledge. For this, a platform is required, such as conference or workshop to interact with each other among various academicians, researchers and industry experts. MITS is able to provide such platforms to the faculty, research scholars and PG students by organizing this National Conference - "Advanced Communication Systems & Applications" with the co-operation of the management and staff members. I appreciate the program coordinator and everyone who is participating and showing enthusiasm in organizing this National Conference. I wish the event a grand success.

[Prof. K. Lal Kishore]

MESSAGE

Sri. N. Vijaya Bhaskar Choudary

M.Com, (Ph.D.)

Secretary & Correspondent

It's my absolute pleasure, getting you through this quote, to excel in your research fields. I take this opportunity to establish the concern HOD and his team of Faculty, an embodiment of enthusiasm who launched this meet to warm you up intellectually superior and to committable destination. I am nostalgic to have perceived the enhanced success this year. It is with the support of such workmanship that rendered their renewable energy to reach out to a wide and diversified success.

"Taking technology for students and making students for technology" is the motto of MITS ever since from its inception. This National Conference will show a better path for academicians, PG & research scholars to integrate modern learning tools and provide ample opportunity to fulfill their career needs. Here with, I extend my warm wishes and accolades to all of them who struggled to see this program at the apex level and aspire to several such platforms for students to kindle their scientific temper.

MESSAGE

Sri. N. Krishna Kumar

M.S (U.S.A)

Chairman

Ensuring you that this assertion is absolutely true, I would like to extend my gesture of appreciation to my well-knit team of the organization. This National Conference helps you to develop on research focus for which the organization has forged useful links with various renounced software electronics and life sciences. Companies and industries in the state are shaping current engineering practices, cutting-edge technologies and emerging trends in the Industry. It is at this level, this program would be an ideal platform for PG and research scholars to display their scientific temper, provides an outlet to the various ideas and postulates that churning success.

In the present sophisticated world of opportunities, at the best of times and in the best of context, we are there to strengthen such programs that empowers work ambience and gets perfect platform to those who want to grow and be in the forefront of the Industry. I wish you all the very best.

MESSAGE

Dr. K. Sreenivasa Reddy

B.Tech., M.E., Ph.D. MISTE, FIE, MIAENG

Principal

This National Conference is intended to bring out a platform for PG scholars, research scholars, academicians and industry experts to exhibit their knowledge and research abilities in the area of Electronics and Communication Engineering. The technological information dissemination to public is the key factor in bringing concerned people and department together. The department of Electronics and Communication Engineering is contributing best of its efforts in development of technical temper by conducting this National Conference. I wish success to all the participants by providing the platform for them to present the research papers.

MESSAGE

Dr. A. R. Reddy

Professor & Head

ECE Department

Developments in Electronics and communication are very important for the progress of the country. Government of India has already released National Electronics Policy – NEP2020 for establishing manufacturing clusters and research centers of excellence. The NEP2020 provides the stimulus for the growth of electronics in the country and provides huge employment opportunities.

MITS, Madanapalle is one of the recognized research centers by JNTUA, Ananthapur and ideally positioned to conduct a National Conference with the sponsorship from TEQIP-II. The proposed National Conference on "Advanced Communication Systems & Applications" is the right step to usher in research developments at MITS, Madanapalle. This platform enables to present the best papers and exchange ideas to conduct research by research scholars, faculties and scientists spread across the country. Research papers of several topics are scheduled for the presentation. The major topics covered in the conference are Communication systems, Embedded & VLSI Technology, Signal Processing, Security Protocols and Encryption systems, WiMax, Wi-Fi, Bluetooth, ZigBee, Mobile cellular system, Satellite Communications, 3G, 4G, LTE and Radar systems.

I wish all the participants a fruitful presentations and cordial discussions at this event.

ABOUT THE DEPARTMENT

The **Department of Electronics and Communication Engineering** was established in the year 1998-99, the department offers B.Tech program in Electronics and Communication Engineering with an intake of 180. It also offers two M.Tech programs Digital Electronics and Communication systems with an intake of 36 and Micro & Nano Electronics with an intake of 18. A team of highly qualified senior faculty runs it with specializations in Communication Systems, Microwave Engineering, Digital Signal Processing, Digital Image Processing, VLSI and Embedded Systems. The main objective of the department, right from its inception, is to train and develop high quality man power, as well as technical inputs primarily to meet the requirements of Indian Industries and R & D establishments both in India and Abroad.

The department is adopting its curriculum, laboratories to stay abreast of Electronics and related areas. The department is regularly conducting the seminars, guest lectures, workshops and technical symposiums on latest technologies. Apart from the curriculum the department is having project development center to impart the real and practical technical skills to the students. The department has been in forefront for research and training activities in Digital Signal & Image Processing, Embedded and VLSI Systems. The following laboratories are operated by the department.

- Electronics Devices & Circuits Lab
- Analog and Digital Communication Lab
- Electronic Circuits Analysis Lab
- Pulse and Digital Circuits Lab
- Linear and Digital IC Applications Lab
- Microprocessor and Microcontroller Lab
- Embedded System Lab
- Digital Signal Processing Lab
- Microwave & Optical Communication Lab
- Digital System Design Lab
- Communication & Signal Processing Lab

Approval for a college to establish a Ph.D. Research Centre denotes excellence in Academic Pursuits. MITS has been recognised as Research Centre for: Electronics & Communication Engineering, Computer Science Engineering and Management Sciences in the year 2013.

PART - A

Session-I(VLSI-Design and Applications)

PART - B

Session-II (Signal & Image Processing)

PART - C

Session-III (Communication Systems & Networks)

Implementation of Genetic Algorithm for the Power consumption in Design of VLSI circuits

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ABSTRACT

Space, power and speed are important issues in VLSI design and Circuit. The component design contradictory influence on the whole Output circuits. Optimization of the power loss can achieve by compromising various components. Consumption VLSI (as in multipliers) and dependent data. In this article, an attempt was made ??to test different design methods and propose a modular approach to energy optimization. It should be noted that the Design is based on an algorithm to reduce the switching input of the gate dramatically activity and, as Cause a reduction in multiplier energy consumption.

Keywords

Genetic Algorithm, Booth Multiplication, Power Optimization.

I. INTRODUCTION

Reducing power dissipation is an important problem in the VLSI design. The design parameters have conflicting effects on the overall system performance. Depending on the component, and based on approaches, different optimization techniques can be accepted. For example, the power Consumption multiplier data dependent contribute more switching activity gate Consumption. The gate circuit activity can be optimized by taking different combinations. Door switch activity can be reduced by using different algorithms. For example in Size design method Multiplication influence performance Consumptions used. Multiplier in addition to primary method school bit multiplication, as Booth algorithm and modified algorithm can be used for efficient propagation.

Design at the gate of the circuit can be used to determine different combination circuit and the associated energy consumption. Genetics Algorithm can be used effectively to explore more combining circuits. Different paper survey approaches energy consumption in VLSI circuits, when testing the multiplier used to study various approaches.

II.A DYNAMICS OF POWER CONSUMPTION

The loss of power in VLSI circuits based on three main sources of power that is necessary to load or unload a node. The power loss due to the output transition power dissipation and due to leakage current. Thus, improvements can be made by the combination of design issues.

Power Consumption can be given by connecting Equation:

$$P_g = fC_{sc}V_{dd}^2 \qquad \text{.....Eq} - 1$$

Where,

P_g = Power consumed by a single gate

f = Average operating frequency of the gate

C_{sc} = Switching capacitance of the gate

V_{dd}^2 Power supply voltage

(Eq-2) is obtained from (Eq—1*);* for any number of gates in the chip.

$$P_g = NfC_{sc}V_{dd}^2 \quad \text{.....Eq –2}$$

Where N f , represent the total number of bit operations per second

POWER DISSIPATION ESTIMATION

In logical circuits, power consumption information on each transfer and inherent system are sending in queries. Where R is the transmission rate for a given architecture, and the lower limit of this rate can be determined, which are thus not used to estimate the power dissipation. Various digital architectures have the same function can also sent different information transfer speeds, and different transmission capacity. Channel Capacity can be specified by:

$$C = \int_0^w \log_2[1+\mathrm{SNR}(f)]df \quad \text{.....Eq -3}$$

Where SNR is the signal-to-noise ratio. Significant transmission capacity should be greater than or equal to A. The overall noise and the performance of digital circuit are the function of a Signal strength, temperature, semiconductor Real estate, etc. However, the power losses mainly due to ground bounce. Lowest related power loss can transfer information that can be calculated by Channel capacity. R is required Transmission of information, W is its bandwidth sigma noise power and C is the Channel capacity. Using (equation 3) and (equation 4), the lower limit of the power loss can give that:

$$P_{D2/\min,ser} = C_L\left(\frac{R}{2W}.1\right)86_N^2 W \quad \text{.....Eq—4}$$

II.B. DATA DEPENDENT POWER OPTIMIZATION

The complexity of the data contributes to the Gate switching input type in the circuit. Through Adoption of the computationally efficient algorithm Components of the circuit design grid Stage can be reduced. The survey of the different designs and arithmetic representations could reduce variations in performance. The model can be built to simulate the energy consumption.

By applying a standard simulation model and comparison with optimum improved design Component can be found. Gate switching in all initial states and all entries can simulation to analyze the electricity consumption at each option. Account of the data dependency is useful in the complexity of the design of the door. Order of inputs for the gate affects both power and deceleration. Analyzed [1] methods describe the optimization of the power and / or the delay of logic gates based on transistor substitution. Therefore, significant improvements in Power and delay can be obtained by appropriate Arrangement of transistors, so late incoming signals are closer to reduce the delays exit.

Another approach to reduce the power size of the grid, which was considered as significant effect on the circuit delay and the loss of power. By increasing the size of gate of transistors within the given gate can be reduced, but on the other hand, due to the power dissipated in the door manufacturing increased. Therefore, an optimal balance can be achieved by sizing the transistors appropriately. One method is to calculate the loss at each gate in the circuit, the Adjuster grid corresponds to the amount of Door can be slowed without affecting the critical delay of the circuit. Alternatively, in various sub circuits softer than zero sub circuits are used and the size of transistors is reduced until the set is zero, or reach a minimum size transistor.

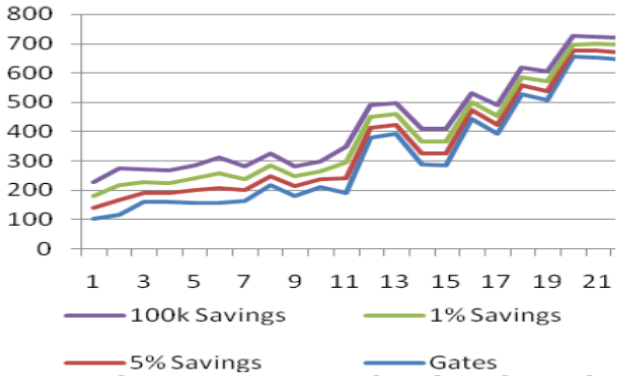
III. COMBINATIONAL GATE LEVEL DESIGN

In the design of gate level circuit, different combination of logic gates can produce the same output circuit, but different Value of the energy consumption. Road balancing the separation and do not care optimization can be used to optimize Consumption. Balancing path can be attained by the avoidance deceleration at each input Gate.

Genetic algorithms can be used to determine different combinations of doors and energy consumption can be formulated developing the fitness function. Coello. al. [3] proposed the design of combinatorial Logic circuit based on the genetic algorithm. According to the definition of the development program chromosomes for various combinations of logic Circuits designed with cross-over and Mutation. This approach is more efficient (in some scenarios and constraints) as human designers such as various restrictions topic will be developed circuit design Fitness function.

To reduce genetic algorithm Number of goals, the associated reduction Energy consumption, as the work of Coello and. al. [2] shows two bit adder and 2-bit Multiplied by a “cardinal” specific [2]; reduction of about 56% in the number of goals for the circuit can be realized.

NUMBER OF GATES VERSUS POWER SAVING IN CMOS – BASED ON ISCAS-89 BENCHMARK CIRCUITS [8]



***(Graph-1) Gate Vs Power based on the work of Jonathan P. Halter and Farid N. Najm* [8]**

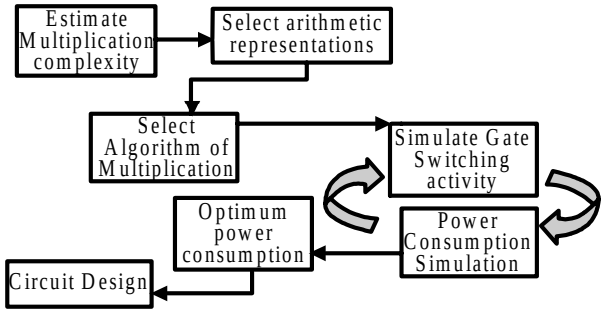
It is very obvious that many circuits dissipated in the door, and manufacturing increased. Therefore, an optimal balance can be achieved by sizing the transistors appropriately. One method is to calculate the loss at each gate in the circuit, the adjuster grid corresponds to the amount of door can be slowed without affecting the critical delay of the circuit. Alternatively, in various sub – circuits where softer than zero are used and the size of transistors is reduced until the set is zero, or reach a minimum size transistor.

(Table-1) Power reduction versus Speed loss

Power Reduction in supply voltage	**Speed Loss**	**Constraints/ Specifications**
Leakage power reductions up to 56%	Not reported	"The logic of design Lower loss of CMOS circuits use clock gating lower dynamic force Power loss tested ISCAS-89 reference circuits " [8]
0.14 V or 810 times	18 times	0.5-fim gate length and static logic **[9]**
"The supply and 1.1V consumes less 5 mW, which is more than three Orders Orders of magnitude lower comparative power Equivalent the commercial register Solutions "[10].	Not reported	----------

IV DISCUSSION

For example, a modular approach is shown in (Fig. 1) has proposed that Careful optimization technique considering various options Design of the multiplier.



(*Fig. 1*) *Modular approach of Multiplier Design*

Complexity in digital level combination of different door Circuits has important implications in forces the loss of power. In addition to the physical design of the chip it can be optimized by genetic Algorithm by analyzing investment option; part of the problems on the program space. Similarly, the choice of algorithm and Booth Modified Booth algorithm can be reduce the energy consumption due to data Complexity. It should be noted that in the multiplier Circuit the modified Booth algorithm reduces energy consumption compared to other Propagation methods.

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Reduction of Coupling Transitions by Using Encoding Techniques in VLSI Circuits

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ABSTRACT

In modern digital circuits the total power attributed to wires is increasing. Reducing the power consumption in wires play a major role in low power design. Coupling transitions contribute to significant energy loss in deep sub-micron buses. Earlier schemes using the switching activity minimization based upon the substrate capacitances are not valid in these buses. Hence, a new low energy bus-encoding scheme is proposed which showed 10 % reduction in coupling transitions for 8 and 16 bit data.

Keywords

Bus,Coupling Transition, Self- Transition, Coding, Decoding.

1. INTRODUCTION

In many digital processors the power dissipation in the bus is a major part of the total chip power dissipation. For CMOS circuits most power is dissipated as dynamic powerfor charging and discharging node capacitances. These capacitances are mainly the substrate capacitances of the bus wires. In these buses the power dissipation due to a transition on a bus wire is equal to P = T a C s V 2 DD f / 2 , where C S is the substrate capacitance, Ta is the transition activity of the bus wire, f is the data transmission rate and VDD is the supply voltage. Several power reduction methods for bus data transfer have been proposed [1,2,3,4,5,6]. All these methods focus on reducing the number of bus transitions. Stan and Burleson employed bus invert coding for a bus whose wires are far apart [1]. In his method, the total number of transitions occurring between the newly arrived data and the present data on the bus is first calculated. If this number is more than half the number of bus wires, then the data is inverted and sent on the bus. Otherwise, the data is sent as is.

As the spacing between wires is getting closer and closer (deep sub-micron technology), the effect of the inter-wire (coupling) capacitances becomes more dominant that it even surpasses the substrate (base) capacitance of a wire. Therefore, in the presence of these coupling effects, earlier methods of power reduction by minimizing the switching activities based only upon substrate capacitance of a bus may not achieve their intended goal. Hence, encoding mechanisms for bus energy reduction that only rely on minimizing the number of transitions are not efficient any more.

The coupling capacitance depends on the switching behavior of a wire by taking into account its neighbors. Consider three wires as shown in Figure 1 with minimum spacing between adjacent wires. The case shown illustrates simultaneous switching on all three wires. The middle wire is shown in bold to indicate that it is switching in one direction (low to high), while the outer two wires are shown in non-bold to indicate their switching in the opposite direction (high to low). In such a case, the effective coupling capacitance gets doubled compared to the case when the neighbors are quiet. On the other hand, if all three wires are switching in the same direction (low to high) as shown in Figure 2, then the coupling capacitance becomes effectively zero.

One of the obvious ways to reduce the coupling capacitance is to increase the distance between adjacent wires, which is in contradiction to deep sub-micron technology. Another way to reduce the coupling effects is

to carefully encode the data before being sent on the bus. Sotiriadis etal have extended the work on encoding bus traffic to account for inter-wire capacitances in deep sub-micron buses by following the latter approach [7,8]. They proposed an encoding technique that attempts to

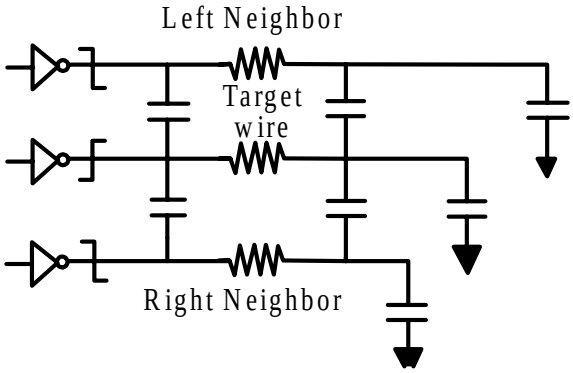

Figure 1 : *Cross coupling effect on the target wire from adjacent wires: Bad case*

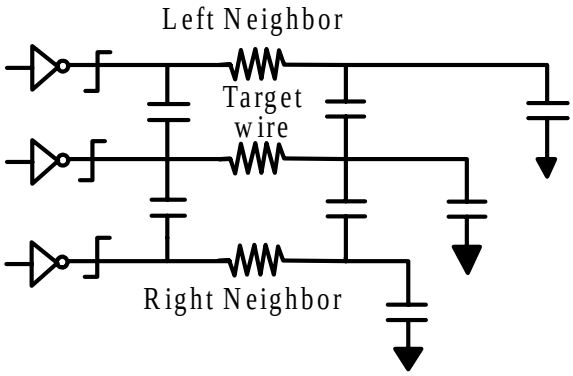

Figure 2 : *Cross coupling effect on the target wire from adjacent wires: Good case*

minimize coupling transitions between bus wires and claimed 40% in energy savings on buses, but ignored the power consumed by the massive and complex encoding and decoding circuitry that would surpass the energy savings by a huge amount. Here, in this paper we propose a bus encoding technique for reduction of energy consumption on on-chip deep sub-micron buses while overcoming the above limitation by reducing the complex encoding and decoding circuitry with a small and simple circuitry with minimum extra power consumption.

2. CODING SCHEME

Our coding scheme is based on the number of coupling transitions occurring on the bus when a new data is to be transmitted. The transitions occurring on a bus are generally classified into two types: self-transitions and coupling transitions. A self-transition is said to occur whenever a bus wire makes a transition from 0 to 1 or from 1 to 0. When this happens the substrate capacitance either charges from 0 to 1 or discharges from 1 to 0.

A coupling transition occurs between two adjacent bus wires, when the charge stored in the parasitic inter-wire (coupling) capacitance gets modified. For a signal transmission through a two-wire bus, all transitions between possible bit patterns and the normalized energy dissipation due to coupling capacitance are shown in Table 1. The value λ is defined as the ratio of coupling capacitance over substrate capacitance. The energy loss caused by the interaction of the lines through coupling capacitance is captured by λ. The energy consumed during a coupling transition is given by:

$$E_C = T.C.\gamma_{DD}^2$$

where Trepresents $0\lambda, 1\lambda$ and 2λ as given in Table 1.

Table 1, Normalized energy dissipation due to coupling capacitance

Bit Pattern	00	01	10	11
00	0	λ	λ	0
01	0	0	2λ	0
10	0	2λ	0	0
11	0	λ	λ	0

In the following analysis we assume m-bit data words. The data word at time instant 'i' is denoted by D(i). The sequence of data words D(0), D(1),…, D(k) are assumed to be independent and uniformly distributed. Let the input data arriving at time instant 'k' is given by: L(k) = {l1(k), l2(k),…, lm(k)}. The probability of the occurrence of the data D(k) is given by

$$P(D(k) = \frac{1}{2m} \forall k_c m$$

When a new data vector *D(k)* λ and 2λ transitions between a pair of adjacent bus wires $\{l_i(k-1), l_{i+1}(k-1)\}$ and the data $\{d_i(k-1), l_{i+1}(k-1)\}$ are given by the k-maps in Figures 3(a) and 3(b) respectively. The Boolean expression for λ transitions simplifies as:

$$si(k) = \overline{li(k-1)}\,\overline{li(k-1)}\,\overline{di(k)}di + (k) + \overline{li(k-1)}\,\overline{li + (k-1)}$$

$$\overline{di(k)}di + 1(k) + li(k-1)li + 1(k-1)di(k)di$$

$$+ 1(k) + li(k-1)li + 1(k-1)di(k)\overline{di + (k)}$$

The total number of λ transitions for the complete bus is

$$S(k) = \sum_{i=1}^{m-1} si(k)$$

Similarly, the Boolean expression for 2λ transitins similifies as:

$$r_i(k) = li(k-1)li+1(k-1)di(k)di+1(k) + li(k-1)li + 1(k-1)di(k)di+1(k)$$

Hence, the total number of 2λ transitions for the complete bus is given by:

$$R(k) = 2.\sum_{i=1}^{m-1} r(k)$$

The total number of coupling transitions occurring on the bus is therefore given by:

$$Q(k) = S(k)+R(k)$$

Since $\lambda >> 1$ in deep sub-micron busses the self transitions on the bus are neglected.

The following procedure (Procedure 1) is now to encode the data and send over the bus:

PROCEDURE 1

1. If the calculated number of transitions Q(k) is more then half the word length then move to the next step. Else, simply pass the data as is,
2. Calculate the Hamming Distance (HD) between the newly arrived data D(k) and the present data on the bus L(k-1) for the even lines and odd lines separately.
3. If the HD for the even lines is greater than that for the odd lines, then invert the even lines of the newly arrived data while keeping the odd lines unchanged and pass it onto the bus.

If the HD for the odd lines is greater than that for the even lines, then invert the odd lines of the newly arrived data while keeping the even lines unchanged and pass it onto the bus.

If the HD's are equal, then invert both the even and odd lines of the newly arrived data and pass it onto the bus.

$l_i(k-1)l_{i+1}(k-1)$ \ $d_i(k)d_{i+1}(k)$	00	01	11	10
00	0	(1)	0	(1)
01	0	0	0	0
11	0	(1)	0	(1)
10	0	0	0	0

(a) λ Transitions

$l_i(k-1)l_{i+1}(k-1)$ \ $d_i(k)d_{i+1}(k)$	00	01	11	10
00	0	0	0	0
01	0	0	0	(1)
11	0	0	0	0
10	0	(1)	0	0

(b) 2 λ Transitions

The above coding scheme adds two extra lines (code bits) to the bus. The value on the bus L(k) at time instant "k" can now be represented as:

$$L(k) = \{L(k), L(k)\}$$

Where $L_D(k)$ and $L_C(k)$ represents the data bit part and the code bit respectively.

3. ENCODING HARDWARE

The encoding hardware consists of four modules as shown in Figure 4. They are:

(i) Coupling Transition Estimator

The coupling transition estimator consists of an estimator and an adder stage. The estimator calculates the coupling transitions. The newly arrived data is compared with the immediate past data on the bus and the number of transitions $s_i(k)$ and $R_i(k)$ for each pair of bus wires is calculated. The adder then accumulate $s_i(k)$ and $r_i(k)$ for the whole bus to generate the total number of coupling transitions Q(k).

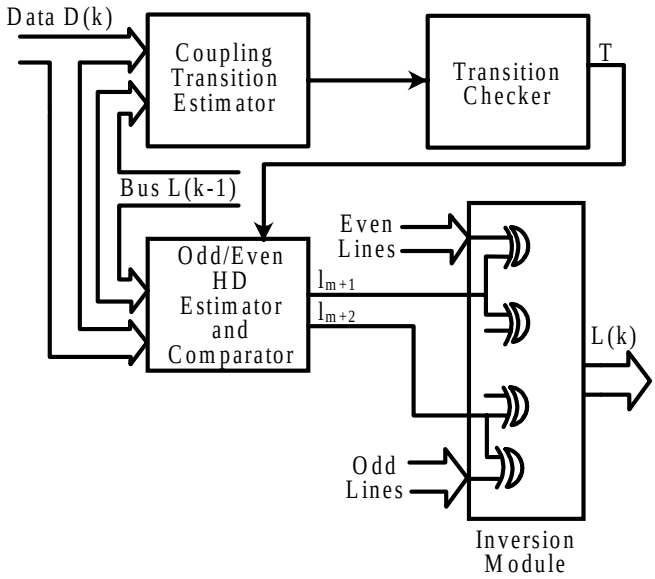

Figure 4 : *Encoding Hardware*

(ii) Transition Checker

The transition checker checks whether Q(k)>m/s. If Q(k) is greater, then it produces a logic '1' at its output 'T', else a logic '0'.

(iii) Odd/Even HD Estimator and Comparator

This module separately calculates the HD between the present state and the next state on the even bus lines and the odd bus lines, and generates two logic signals EV and OD to indicate the relative magnitude of the two values, as given in table 2. A combinational logic circuit then generates the two outputs $l_{m+1}(k)$ and $l_{m+2}(k)$ using the following

Boolean relations :

$$l_m+1(k)=\overline{TOD} \text{ and}$$

$$l_m+2(k)=\overline{TEV}$$

The above two outputs from the code bit part of the bus equations and are transmitted on the extra bus wires of the bus.

Table 2. *Odd/Even HD estimator and comparator*

EV	OD	
0	0	Equal HD
0	1	HD on odd lines greater
1	0	HD on even lines greater
1	1	Undefined

(iv) Inversion Module

This module decides law the data will be transmitted on the bus. If The Transition checker output T is zero, then the new data is transmitted as is. Else, the data will be inverted and transmitted accordingly to Table 3. The code bits $Lc(k)=\{l_m+1(k), l_{m+2}(k)\}$ control this module.

Table 3. Coding of extra bus lines

$l_{m+1}(k) l_{m+1}(k)$		Bus Inverted
0	*0*	*No inversion*
0	1	Even Lines
1	0	Odd Lines
1	1	Both Even and Odd lines

Hence this module consists of set of Exclusive OR(XOR) gates controlled by the code bits l_{m+1} and l_{m+2}.

4. AN ILLUSTRATIVE EXAMPLE

To illustrate out coding scheme consider a 16 bit data (1100, 9910, 1000, 0111), while is presently on the bus. If the next data (1010, 1001,0011, 0101) is sent as is, we have a total of 14λ coupling transitions (Q(k)). Since Q(k) is more than half the word length (8), the data will be encoded using out method. In this case, the number of transitions on odd line of the bus (6) exceeds that on the even lines (3), (In determining the odd/even lines, the least significant bit is counted as number zero.) So the odd bits of the data are inverted (even bits stay the same) and sent through the bus with the additional two lines appended (10,0000,0011,1001,1111). The additional two bits are appended so that the decoder can decode accordingly as specified in Table 3. For this example it may be noted that R(k) = 6 while S(k)8. By applying our coding scheme we have reduced new R(k) to 0 and S(k) to 2. The total number of transitions Q(k) for unencoded and encoded data are 14 and 2 respectively. Hence, we see that the total number of coupling transitions is reduced from 14λ to 2λ, thereby reducing the power consumption.

5. PERFORMANCE EVALUATION

We have evaluated the effective of our coding scheme using a MATLAB program. The simulations used 8 and 16 bit ransom data with 1000 data vectors. Figure 5 shows 8 bit simulations results our technique.

The reduction in the number of transitions achieved is very close to that in the original bus invert coding technique, that took into account only self-transitions, whereas our is a dominant factor in deep sub-micron buses. Simulation results show that about 10% reduction in coupling transitions is achieved by our technique.

6. CONCLUSIONS

We proposed a new coupling driven data encoding scheme for low power data transmission in deep sub-micron buses. The simulation results show that our technique reduces 10% of the coupling transitions for a deep sub-micron bus compared to the conventional non-coded data transmission. As this method is adaptive, it reduces signal transmission for all sorts of data streams.

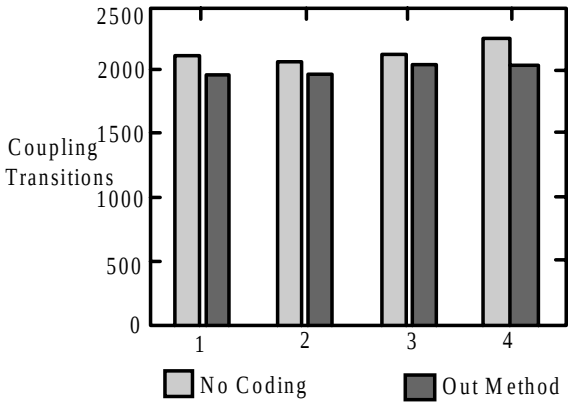

Figure 5 : *Coupling transitions for 8-bit data vectors*

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FPGA Based Design of Customized DWT Using Flexible MAC Operations For Signal Processing Systems

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ABSTRACT

Abstract: In the signal processing systems like video processing systems or spee processing systems , DWT performs the major role to compute the specified tas... A DWT consists of filter stacks. These filter stacks are the sub-modules of filter bank where a pair of HPF, LPF are embedded in it. In any analog defined tool like MATLAB, to construct DWT, predefined HPF, LPF functions will be used. So that, optimized DWT cannot be designed by the designers. Hence, in signal processing as HPF,LPF are designed with floating point multiplier, adder and shifter using convolution or MAC operations; user can change the characteristics of HPF,LPF by changing the parameters of above floating point multiplier, adder and shifter to speed up the process, so that HPF, LPF could be optimized; hence, DWT can be optimized. As DWT is optimized, total signal processing system will be optimized.

Key words

signal processing systems, DWT, HPF, LPF, MAC operations, MATLAB, HDL modeling.

I. INTRODUCTION

For many signals, the low-frequency content is most important part. It gives the signal its identity. The high-frequency content, on the other hand, provides the add on properties to it. Eg. in a human voice if high-frequency components are removed, the voice sounds different, but, if enough of the low-frequency components are removed the complete signal may be lost. In wavelet analysis, approximations and details are the parameters to be obtained. The approximations are the high-scale, low frequency components of the signal. The details are the low-scale, high frequency components. The original signal, S, passes through two complementary filters and emerges as two signals. If the operation is performed on the real digital signal, twice the number of data samples is obtained. Eg. If an original signal S consists of 1000 samples of data. Then the resulting signals will each have 1000 samples, for a total of 2000. These signals A and D are interesting, but 2000 values were obtained instead of the 1000. Performing carefully at the computation, only one point out of two in each of the two 2000-length samples is sufficient to get the complete information. This is the notion of down sampling. This result in two sequences called cA and cD.

The decomposition process can be iterated, with successive approximations being decomposed in turn, so that one signal is broken down into many lower resolution components. This is called the wavelet decomposition tree. The wavelet decomposition tree can be obtained by the implementation of a chain of High pass and low pass filter banks as given below.

II. DESIGN OF DISCRETE WAVELET TRANSFORM

The input sampled signals having 16 bit each are applied in parallel to sub band mapping module after the 12th sample passes to FIFO input unit four sampled signal signals are passed down to input buffer as a packet. Input FIFO stores 12 samples of sampled signal each in which samples are represented in 16 bit floating point notation. After every 12 samples stored in FIFO first 4 samples are passed from FIFO to the input buffer and then fed to the sub-band filter

bank block through the wavelet decomposition. This sub-band carries out filter decomposition of the given input signal of the length 4 samples, considering a bank of Low Pass Filter and High Pass Filter. The filter takes 4 filter coefficients for LPF and HPF obtained from db4 wavelet with the length of 4, which were derived from Matlab. Convolution operation takes on input signal with filter coefficient to obtain detailed and approximate coefficients after down sampling by 2. Each sub-band carries 3 points for passing of every 4 samples. A total of 9 points are obtained for 12 samples passed in each sub-band thus this sub-band unit mapping carries out wavelet decomposition using wavelet filter bank in to 4 sub-bands each sub-band with 9 points. Obtained sub-band samples are stored in sample RAM & its corresponding energies are calculated by the energy calculator module and stored in energy RAM. Scale factor for the sub-band is the sample with maximum amplitude in the sub-band obtained from the comparator module where the comparator module compares all the sample of each subband and find the maximum of it.

III. MODELING OF DISCRETE WAVELET TRANSFORM USING MAC

The filter logics are realized using MAC (multiply and accumulate) operation where a recursive addition, shifting and multiplication operation is performed to evaluate the output coefficients. The recursive operation logic is as shown below.

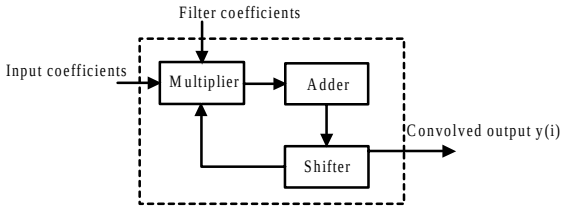

Figure 1 : *Realization of recursive MAC operation*

Before passing the data to filter bank the fifo logic realized stores the data in asynchronous mode of operation, operating on the control signals generated by the controller unit. On a read signal the off-centered data is passed to the buffer logic. The fifo logic realized as shown below.

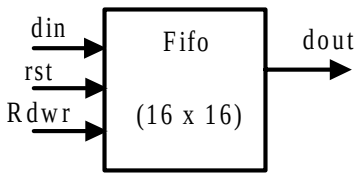

Figure2 : *Realization of 16 x 16 fifo logic for coefficient interface*

The obtained detail coefficients are down sampled by a factor of two to reduce the number of computation intern resulting in faster operation. To realize the decimator operation comparator logic with a feedback memory element is designed as shown below.

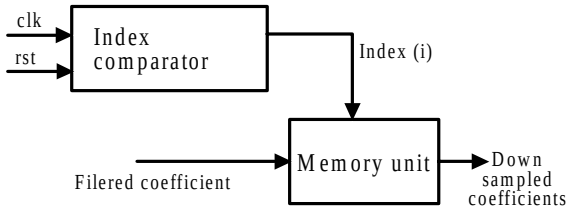

Figure 3 : *Architecture for decimation by 2 logic*

IV. IMPLEMENTATION OF DWT USING VHDL

The proposed system is realized using VHDL language for it's functional definition. The HDL modeling is carried out in top-down approach with user defined package support for floating point operation and structural modeling for recursive implementation of the filter bank logic. For the realization a package is defined with user defined record data type as

```
type  real_single is
  record
    sign : std_logic;
     exp: std_logic_vector(3 downto 0);
    mantissa: std_logic_vector(10 downto 0);
end record;
```

The floating notation is implemented using 16 bit IEEE-754 standards as presented below.

Sign. (1)	Exp. (4)	Mantissa (11)

The floating-point addition, multiplication and shifting operation are implemented as procedures in the user defined package and are repeatedly called in the implementation for recursive operation. The procedures are defined as;

procedure shifftl (arg1: std_logic_vector;arg2: integer;arg3 :out std_logic_vector);

procedure shifftr (a:in std_logic_vector; b:in integer;result: out std_logic_vector);

procedure addfp (op1,op2: in real_single;op3: out real_single) ;

procedure fpmult (op1,op2: in real_single;op3: out real_single) ;

for performing the convolution operation, filter coefficients are defined as constant in this package and are called by name in filter implementation.

```
constant lpcof0:
real_single:=('1',"0100","00001001000");
constant lpcof1:
real_single:=('0',"0100","11001010111");
constant
lpcof2:real_single:=('0',"0110","10101100010");
constant lpcof3:real_single:=
('0',"0101","11101110100");
constant hpcof0: real_single:=
('1',"0101","11101110100");
constant
hpcof1:real_single:=('0',"0110","10101100010");
constant
hpcof2:real_single:=('1',"0100","11001010111");
constant
hpcof3:real_single:=('1',"0100","00001001000");
```

Using the above definitions the filters are designed for high pass and low pass operation. The recursive implementation is defined as;

```
for k in 1 downto 0 loop
        old(k):=shift(k);
fpmult(old(k)(0),hpf(k+1),pro(k)(0));
        proper(j,k):=pro(k)(0);
addfp(acc(k)(0),pro(k)(0),acc(k)(0));
      acer(j,k):=acc(k)(0);
shift(k+1):=shift(k);
end loop;
```

for the evaluation of the implemented design the test vectors are passed through the test bench generated from Matlab tool. The continuous output of secondary side transformer obtained after impulse test are discretized using matlab tool where each coefficient is converted to 16-bit floating notation and passed to the test bench for HDL interface. The coefficients obtained from the filter bank after convolution is then compared with the results obtained from the matlab decomposition for accuracy evaluation.

```
library ieee;
use work.math_pack1.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_1164.all;
entity topmodule_wb is
end topmodule_wb;
architecture TB_ARCHITECTURE of topmodule_wb is
component topmodule
      port (
            clk : in std_logic;
            rst : in std_logic;
            start : in std_logic;
            read1 : in std_logic);
      end component;
signal STIM_clk : std_logic;
      signal TMP_clk : std_logic;
      signal STIM_rst : std_logic;
      signal STIM_start : std_logic;
      signal STIM_read1 : std_logic;
      signal WPL  : WAVES_PORT_LIST;
      signal TAG  : WAVES_TAG;
      signal ERR_STATUS: STD_LOGIC:='L';
  begin
        CLOCK_GEN_FOR_clk: process
      begin
      if END_SIM = FALSE then
            TMP_clk <= '0';
            wait for 50 ns;
             else
            wait;
            end if;
            if END_SIM = FALSE then
                  TMP_clk <= '1';
                  wait for 50 ns;
            else
            wait;
            end if;
      end process;
ASSIGN_STIM_clk: STIM_clk <= TMP_clk;
ASSIGN_STIM_rst: STIM_rst <=
WPL.SIGNALS(TEST_PINS'pos(rst)+1);
ASSIGN_STIM_start: STIM_start <=
WPL.SIGNALS(TEST_PINS'pos(start)+1);
UUT: topmodule
      port map(
            => ,
```

```
clk => STIM_clk,
rst => STIM_rst,
start => STIM_start,
 => ,
 => ,
read1 => STIM_read1,
 => );
end TB_ARCHITECTURE;
end TESTBENCH_FOR_topmodule;
```

V. SIMULATION RESULTS

The DWT has been designed by the user defined floating point multiplier, adder and shifter instead of using the predefined functions. To evaluate the suggested design an analog signal is taken and processed, the observations obtained are as illustrated below,

Samples Considered

0————————- “0000000000000000”
-3.0518e-05————“1000110000110101”
-3.0518e-05————“1000110000110101”
0————————- “0000000000000000”
-6.1035e-05————“1000010000110110”
0————————- “0000000000000000”
-6.1035e-05————“1000010000110110”
-7.1553e-05————“1000011001001111”
-6.1035e-05————“1000010000110110”
-6.1035e-05————“1000010000110110”
-7.1553e-05————“1000011001001111”
-7.1553e-05————“1000011001001111”
-7.1553e-05————“1000011001001111”
0————————- “0000000000000000”
-7.1553e-05————“1000011001001111”
-6.1035e-05————“1000010000110110”
-7.1553e-05————“1000011001001111”
-3.0518e-05————“1000110000110101”
-6.1035e-05————“1000010000110110”
-3.0518e-05————“1000110000110101”
-6.1035e-05————“1000010000110110”
0————————- “00000000000000000”

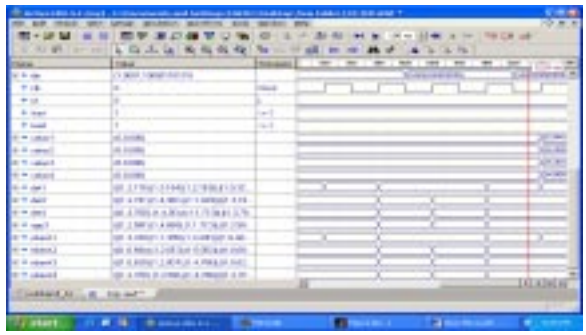

Figure4 : *Simulation result for the implemented subband design*

The top module has been simulated using ModelSim6.1 SE simulator. Figure 4 shows the input values passed to the sub-band module. The inputs are passed to the module in Floating point Excess-7 notation. The system is passed with a clock of 100Mhz system application frequency with reset signal low as the system considered being active low. The Signal ‘start’ and ‘read’ is fed high for making the system enable and to read the data from the buffer element. The result shows the scale factor obtained for each sub-band. The signal ‘det1’,’det2’,’det3’ and ‘app3’ gives three detailed coefficients and approximate coefficients for the input signal. Each sub-band constitute of 9 sub-samples for every packet of the data burst. The ebank’s gives the energy values of each subband sample for each subband

Figure.8 also shows the overall scale factors, detail coefficients and approximate coefficients for every packet of the signal samples. The scale factors obtained show the maximum values of the sub-band samples obtained under each subband. The energy for the samples are calculated as E = square (Magnitude of each sample).

The elements of the detailed coefficient matrix (det1) show the samples lying in the higher frequency range from 8-4KHz. The second sub-band shown by (det2) gives the coefficients lying in the range of 4-2 KHz ranges. Det3 gives the sub-samples with a frequency of 2-1KHz and app3 matrix shows the approximate coefficients lying in the range of 1-0KHz ranges .

The VHDL design of the DWT has been synthesized using XILINX ISE tool. Figure5 shows the logical routing of the implemented design targeting on to Xc2s50e-ft256-7 FPGA of virtex family. The routing is carried out on Xilinx FPGA editor. The result obtained shows the real time FPGA interconnection of logics connected inside the FPGA.

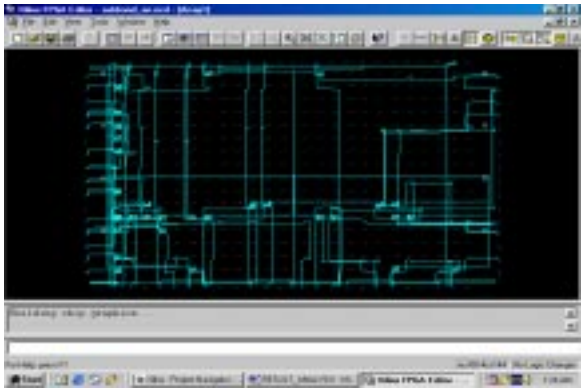

Figure 5 : *Routing of the implemented wavelet decomposing module targeting to Xc2s50e-ft256-7*

The synthesis report for VHDL design of DWT using optimized HPF,LPF has been shown in the below statements.

Minimum period: 2.649ns

(Maximum Frequency: 377.501MHz)

Minimum input arrival time before clock: 9.656ns

Maximum output required time after clock: 6.366ns

Design Statistics

IOs : 105

Cell Usage :

BELS : 205

VI. CONCLUSION

This paper outlines the design of a DWT using VHDL for the optimization. The DWT has been customized using user defined floating point multiplier,adder and shifter. Hence, the flexibility is very high to increase the speed of operation of DWT so that the speed of operation of a signal processing system will be increased. The proposed design implements a general purpose Fast Wavelet transformation system which gives rise to accurate sub-band decomposition of the signal into four distinct sub-bands. The scale factor for each subband is also obtained with the energy of each subband samples been calculated. From the obtained result plots it is observed that the retrieved signal samples show less variation from the input.The proposed design is completely developed on a ModelSim 6.1SE tool using VHDL language and has been synthesized on Xilinx ISE tool targeting to Virtex FPGA. The system implemented is attained for a Minimum period: 2.649ns i.e. a Maximum Frequency: 377.501MHz. Hence, it is concluded that the development of DWT using user defined floating point arithmetic is so flexible than predefined functions..

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A Low - Power Wearable Physiological Parameters Monitoring System

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ABSTRACT

The design and development of a low power wearable physiological paramete monitoring system have been developing and reporting in this paper. The system can be used to monitor physiological parameters, such as ECG signals, and temperature. The system consists of an electronic watch which is worn on the wrist and arm, by an at-risk person. An epic sensor has been used to detect ECG signals. The device stores the ECG measurement of a patient and continuous reading takes place by interfacing with computer. The device is battery powered for use anywhere. The device can be easily adapted to monitor athletes and infants. The low cost of the device will help to lower the cost of home monitoring of patients recovering from illness.

Index Terms

Body temperature measurement, ECG signals, wireless transmission, sensors, physiological parameters, Radio frequency.

I. INTRODUCTION

In recent times, wireless sensors and sensor networks have become a great interest to research, scientific and technological community. Though sensor networks have been in place for more than a few decades now, the wireless domain has opened up a whole new application space of sensors. Wireless sensors and sensor networks are different from traditional wireless networks as well computer networks and , therefore, pose more challenges to solve such as limited energy, restricted life time,etc.

Wireless sensing units integrate wireless communications and mobile computing with transducers to deliver a sensor platform which is inexpensive to install in numerous applications. Indeed, co-locating computational power and radio frequency (RF) communication within the sensor unit itself is a distinct feature of wireless sensing. Today, the progress in science and technology offers miniaturization, speed, intelligence, sophistication, and new materials at lower cost, resulting in the development of various high-performance smart sensing system. Many new researches is focused at improving quality of human life in terms of health by designing and fabricating sensors which are either in direct contact with the human body or indirectly. One of the reasons for more development in this area is the global population and rise in ageing population, one statistic provided by the U.S Department of Health that by 2050 over 20% of the world's population will be above 65 years of age. This results in a requirement for medical care, which is expensive for long-term monitoring and long waiting lists for consultations with health professionals. The cost of hospitalization is ever increasing, so is the cost of rehabilitation after a major illness or surgery. Hospitals are looking at sending people back as soon as possible to recoup at home. During this recovery period, several physiological parameters need to be continuously measured. Hence, telemedicine and remote monitoring of patients at home are gaining added importance and urgency.

This system has been designed with sensors, host computer. The system consists of a temperature sensor, epic sensor, a micro controller, and a low-power transceiver.

It records temperature and ECG pulses for 24 hours. These data are transmitted to the computer by using radio frequency, the records can be saved. The reported systems are expensive and the cost depends on the number of sensors used. The reported device consists of a wrist and arm and the msp430 microcontroller unit connected with arm band. Ambulatory EKG monitoring can also be a useful tool in monitoring elderly people, perhaps in a care-home setting or via telemedicine, to alert their carers to heart-related problems at the earliest possible opportunity. Rapid response to cardiac arrest or stroke events can have an enormous impact on the ensuing quality of life, or even be the difference between life and death. When combined with sensors measuring other vital signs the resulting system can do much to extend the all-important independence of the elderly.

There are currently three main electrode types used for ambulatory ECG recording, Ag/AgCl stick on electrodes, with contact enhancing gel; plastic electrodes as found in chest straps; and textile electrodes, used in wearable systems. All of these electrodes rely on a good galvanic contact to the skin, as the coupling to EKG amplifier is resistive. All of these sensors are to some degree invasive – in the case of Ag/AgCl electrodes the gels and adhesive can cause skin irritation, and chest straps can be difficult to fit, uncomfortable to wear and not always reliable.

II. SYSTEM OVERVIEW

Fig. 1 shows the functional block diagram of the system hardware. The system has been designed to take several inputs to measure physiological parameters of human such as temperature, ECG. The inputs from the sensors are integrated and processed. The results are sent through RF module to a host computer, which stores data into a database. The values can then be displayed on the Graphical User Interface (GUI) running on a computer. Once the user has connected to the receiver unit, data is automatically updated on the screen. Temperature and ECG are display on the screen. The data plotted on a time graph which can be customized to show data received from any of the sensors.

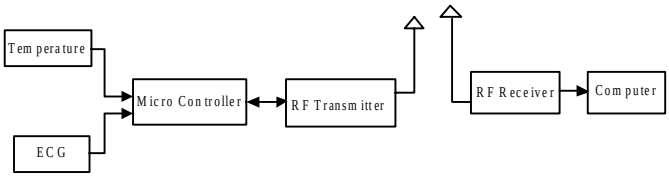

Fig 1: *Block diagram of Physiological parameter monitoring system*

The design is modular which makes it rather easy and straight forward to add extra sensors for measuring and monitoring other parameters.

III. DETAILS OF THE SENSING SYSTEM

The current version of the system consists of two sensors: a temperature sensor, EPIC sensor. Temperature sensor circuitry used in the design generates analog voltage which is fed to the analog-to-digital inputs of the microcontroller. The ADC input is time-multiplexed and sampled at different rates.

A. EPIC SENSOR

EPIC is an acronym of Electric Potential Integrated Circuit. The EPIC sensor is thus an electrometer capable of measuring AC electric fields or potentials. The device has very high input impedance and requires no ohmic contact to the source being measured as its input is capacitively coupled. It can be thought of as being close to the ideal voltmeter, able to measure electrical signals whilst taking virtually no energy from the system being measured.

A block diagram showing the basic construct of the sensor is shown in figure 2.

The key features are the two feedback paths: guarding, which drives the guard to the input potential and so minimizes the input capacitance and bootstrapping which can be used to increase the input impedance. The sensors are currently produced with either x10 or x50 gain, with a bandwidth of the order of 50mHz to 30Khz.

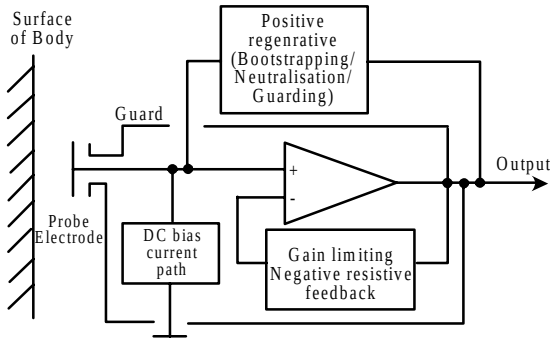

Figure 2: *Block diagram of a typical EPIC sensor*

All of this makes EPIC well-suited to measuring a wide range of electrical signals, including electrophysiological signals, such as the electrocardiogram (EKG or ECG) from the heart, electromyogram (EMG) from muscles, electro-oculogram(EOG) from the eyes, and electro-encephalogram (EEG) from the brain. The EPIC sensor's ability to measure various electrophysiological signs has been documented by Plessey's partners at the University of Sussex.

Because of the large coupling capacitance to the body (around 250pF) the EPIC sensor's internal electro-

meter can be used in differential mode to recover true surface potential ECG signals from the surface of the skin. A typical ECG signal at the surface of the skin is 1mV p-p.

EPIC's real advantage – compared to other sensors in this field – lies in its capacitive coupling to the source being measured. Some of the issues with other sensor types have already been mentioned in section 1, but because EPIC does not rely on an ohmic contact to the skin, there is no need for skin preparation or contact enhancing substances. Depending on the system requirements and the strength of signal being measured, it is possible to measure high quality electrophysiological signals through multiple layers of insulating materials (e.g. clothing).

There is a need to ensure zero, or at least the very minimum of, movement between the sensor electrode and the human body, and this is perhaps the greatest technical challenge in the system presented here.

B. ELECTROCARDIOGRAM (EKG)

Many readers will be familiar with the science of the electrocardiogram, but a brief overview here will help in understanding the challenges presented in developing a single-arm EKG measurement system. Work at the end of the 19th Century and in the early 20th Century first discovered and then characterized the electrical activity of the heart. A famous diagram produced by Waller in 1887 shows the electric field across the thorax produced by the dipolar source that is the heart.

By placing sensors at various points on the human body it is possible to measure different electrical vectors, and so determine very detailed information about the health of the heart. Essentially to achieve a good electrical cardiac signal it is necessary to measure the differential electrical signal between two points, one either side of the heart. The use of a pair of sensors to generate a differential measurement is key to any EKG system using EPIC sensors as this provides good common mode noise rejection. As already stated the EPIC sensor measures electric fields, and the strongest field that will be detected on a person inside most buildings will be the 50 or 60Hz that is coupled onto the body from the mains electricity supply. This signal will typically have amplitude of several volts on the EPIC output, compared to tens of mV for the wanted EKG signal. By using a pair of sensors and a differential amplifier with good common mode rejection, along with some basic analog and digital filtering, it is relatively straightforward to extract the EKG component from the large noise signal. The basic hardware system architecture is shown in figure 2.

The earliest systems built using Plessey's EPIC sensors concentrated on measuring the Lead I EKG (left arm to right arm), taking one contact point on each hand. The arms effectively act as resistive conductors that connect to the positive and negative sides of the heart. A lead I EKG measured in this way is shown in figure 3.

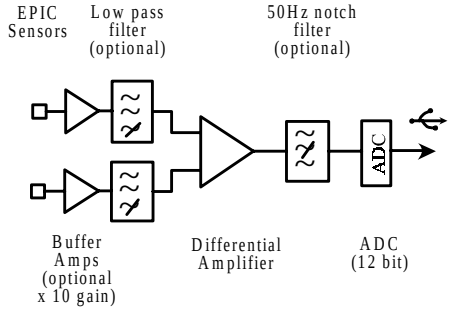

Fig 3: *Hardware system architecture*

The buffer amps on the individual channels have switchable x10 gain and 1st order 30Hz low pass filters. The differential output has a switchable notch filter offering around 50dB of rejection at the mains frequency.

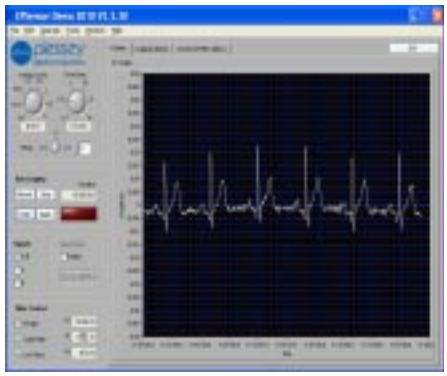

Fig 4: *Lead I ECG measured using hand held EPIC sensors and displayed on Plessey's EPIC demo software. Note that a small amount of EMG noise from the muscles in the arms is also visible on the trace.*

This approach allows a number of practical implementations of EPIC-based EKG sensing systems, including a small portable wireless unit; a wrist watch with two sensors, one of which rests against the wrist of one arm, whilst a finger from the other hand touches the second; and a pair of sensors built into a Smartphone.

The desire for a continuous ambulatory EKG monitor requires that the user is able to "wear" the system such that it will function without needing to occupy one or both hands. As already stated, chest straps that are produced by sports watch manufacturers can achieve this, but in a way that is not always easy, convenient or comfortable.

The system presented here uses two sensors contained within a single armband that can be fitted and

worn relatively simply. The experimental system used two PS25201 sensors, along with Plessey's EPIC demo kit, which consists of an interface box containing some analog filtering, amplification and an analog to digital card with a USB output. The signals were viewed and captured using the lab view interface software developed for EPIC that is also part of the standard demo kit.

The PS25201 sensors have 50x voltage gain and are packaged in a metal can. The front surface of the sensor consists of a 20mm diameter electrode with a TiO2 dielectric face, surrounded by a metal ring that is at the system ground (0V). When pressed against the arm both the electrode and the ground ring make contact with the skin.

The sensors can be seen in figure 5, which shows the two sensors mounted onto a sports armband.

These applications meet the need for a very easy to use monitor that can be used on an *ad hoc* basis to record relatively short periods of EKG activity.

Fig 5: *PS25201 sensor mounted on a Sports Arm-Band*

C. TEMPERATURE SENSOR

The temperature is measured inside the watch right inside the CC430 device. When the watch is worn, the temperature of the watch may be different due to the body heat. For accurate temperature measurements, do not wear the watch and allow a sufficient amount of time for the watch to adapt to the surrounding temperature.

IV. MICRO CONTROLLER

The eZ430-Chronos software development tool is a highly integrated, wearable, wireless development system that is based on the CC430F6137. It may be used as a reference platform for watch systems, a personal display for personal area networks, or as a wireless sensor node for remote data collection.

Based on the CC430F6137 sub-1-GHz RF SoC, the eZ430-Chronos is a complete development system featuring a 96-segment LCD display, an integrated pressure sensor, and a three-axis accelerometer for motion sensitive control. The integrated wireless interface allows the eZ430-Chronos to act as a central hub for nearby wireless sensors such as pedometers and heart-rate monitors. The eZ430-Chronos offers temperature and battery voltage measurement and is complete with a USB-based CC1111 wireless interface to a PC.

The eZ430-Chronos watch may be disassembled to be reprogrammed with custom applications and includes an eZ430 USB programming interface.

Figure 6 shows that the block diagram of ez-430 chronos device.

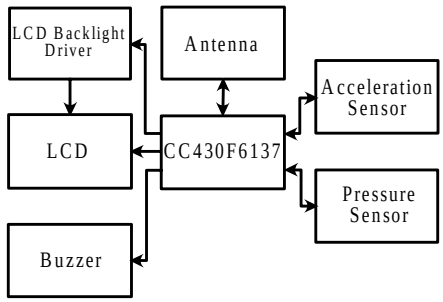

Fig 6: *eZ430-Chronos Watch Block Diagram*

V. COMMUNICATION

The communication range that can be achieved in a radio system depends very much on the antenna solution. It is important to understand the difference between different antennas, and the tradeoffs to be made, in order to select the right antenna solution for a particular application.

In many SRDs (Short Range Devices) the physical size is restricted, and hence the antenna ought to be small as well. The important aspects of small antenna design are presented in this application note. Several PCB integrated antenna solutions are shown, and a practical design.

For long-range systems requiring high efficiency antennas, external resonant antennas must be used. An overview of these kinds of antennas is also given. Applications involving body-worn or handheld devices represent a special challenge for the antenna design. In the end of this note these problems are addressed.

The RF access point allows wireless communication with the eZ430-Chronos directly from the PC to download data, sync information, or control programs running on the PC It is based on the CC1111F32 controller, which features an integrated USB controller in addition to a <1-GHz radio. The access point is this kit comes in a small production-ready design. Therefore, it does not include a JTAG connector. However, the bottom side provides pads that allow soldering cables to connect the CC1111 to the CC Debugger.

The access point is designed to be production ready and as small as possible. Therefore, no debug connector is added. However, it may be reprogrammed by attaching a TI low power wireless debug interface to the corresp-

onding pads on the bottom side of the PCB. Figure 7 shows that the eZ430-Chronos RF Access Point.

Figure 7. *EZ430-Chronos RF Access Point*

VI. FURTHER WORK

The system presented here demonstrates proof of concept of an ambulatory EKG system and has illustrated the importance of choice of sensor location, and the advantages to be gained by incorporating a closed loop driven ground system.

There are many further improvements that could be explored and implemented to improve noise

Immunity and signal quality. These include the following.

EKG vector study. As has been shown, the positioning of the sensors around the arm gives access to a number of different vectors from the heart, in much the same way as different vectors are viewed in 12-lead EKG systems. To the best of the authors' knowledge, single arm EKG signals have not been widely explored to date, and there is potentially much to be gained by studying correlations between conventional leads and what can be measured on a single arm.

EMG Study, as mentioned previously, characterization of the signals produced by the arm and shoulder muscles during various arm movements would enable better decisions to be made on positioning of sensors and removal of EMG noise.

Electrode design. The rigid metal and titanium oxide electrodes on the standard EPIC sensors do not conform well to the contours of the human arm. Plessey have experimented with some success on the use of conductive fabric electrodes in other EPIC applications, and it is anticipated that forming electrodes from a combination of conductive and insulating fabric could produce a system that both gives better results and is more comfortable to wear.

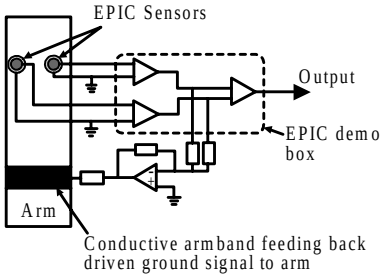

Figure 8 : *Block diagram showing addition of driven ground circuit to minimize noise due to static charge build up.*

Software. The data presented here are filtered using basic DSP techniques. Further software processing developments such as averaging to remove base line wandering, filtering using wavelet transforms and so forth could potentially do much to improve the basic signal.

Multiple sensor system. As described earlier, the optimum sensor location for a two-sensor system can be a compromise between best signal strength and EMG rejection, and by using multiple sensors it may be possible to remove this compromise. Furthermore, data collected to date suggest that it may be possible to gain more information on the heart by viewing an untilled system.

Driven Ground. The driven ground circuit used for this work was developed and optimized for a Non-contact EKG system rather than for the single-arm contact EKG application. The current system is able to maintain good data from a subject who is walking, but with further refinement of the techniques, a system is envisaged that can cope with a subject engaged in vigorous exercise such as running.

VII. CONCLUSION

A system has been presented for ambulatory EKG monitoring using capacitive sensors mounted on a single arm. By careful positioning of sensors and the use of a driven ground, the design presented here demonstrates that a practical single arm EKG solution can be built using Plessey Semiconductors' EPIC sensors. Ideas for future improvements to the system have been suggested.

VIII. REFERENCES

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[2] Plessey Semiconductors' Application note: Noncontact ECG measurement using EPIC. Web:www.plesseysemiconductors.com/doc/?id=291566 (Visited 15:00, March-13, 2013)

[3] Texas Instruments ez-430 chronos device as a micro controller http://processors.wiki.ti.com/index.php/EZ430-Chronos

A New Generation Automatic Tracking and Monitoring a person Using FPGA Core

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ABSTRACT

Automatic a Person Tracking is a system, where a person or an commodity can be tracked using devices that are integrated with Global positioning System (GPS) and Global Service for Mobiles (GSM).

*When people talk about a "GPS," they usually mean a "**GPS receiver**". The U.S. military developed and implemented this satellite network as a military navigation system but now let's everyone use the signals. These projects can be implemented with hardware **designed in VLSI FPGA system using Verilog/VHDL.** If a person becomes any important to provide them security and contact someone in case of emergency. Device can be programmed in such a way that, it one touch dial but-ton (SOS) will **send alerts call and voice message** in case of emergency and you can reach to help your loved once. Errant teenagers will regard them with horror, Automatic location tracking services designed to keep tabs on their offspring can give peace of mind.*

Keywords

***FPGA** controller kit, GPS &GSM modems, LCD Display, Android mobile;*

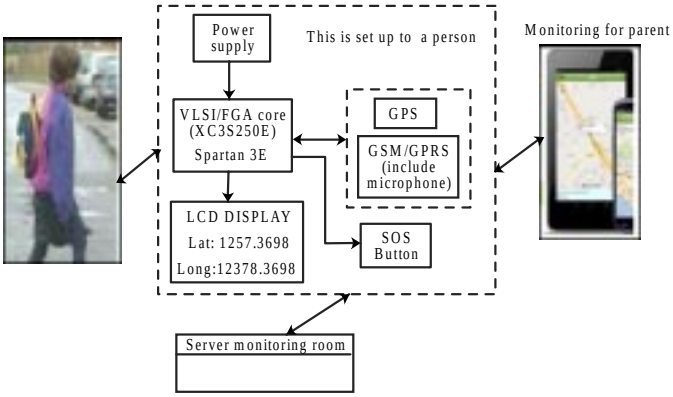
The system has the following requirements.

* Easy to implement and add functions
* Able to manage many children efficiently
* Adaptive for mobility of children who walk from [home school]
* Secure against suspicious individuals
* Low cost
* Portable size

INTRODUCTION

A New generation automatic tracking and monitoring a person is very helpful. The main intention is **to overcome child kidnapping ,women harassments, mentally disorder people and e.t.c** In this Project, person activities are programmed in FPGA core by using Xilinx ISE12.0 version and program is developed by VHDL/verilog code, it is always interfacing with GPS and GPRS/GSM module, if a person arrives in desired location it automatically send a SMS to the receiver(monitor person/parent) as well sends the current address location and shown in a g-map(Google map) by using Android Apps.Into that default programmed the tracks. If person exceeds/avoiding the desired location automatically give alarm to monitor person. So that monitor person no need to check and show their mobiles always. It also provides security and ability to contact our dear one in case of emergency to them by pressing of SOS button. Device can be programmed in such a way that, it's one touch dial SOS button will send you alerts message and call to monitor persons (parent) in case of emergency, monitoring person can help their loved once and, if person is avoid the desired track automatically give alarm to monitor person for quick alert and also send message of its exact location. When monitor person easy to know about their loved once and take action in time, so that over come from danger. This project gives indirectly known information about a person.

BLOCK DIAGRAM



WORKING PROCEDURE

Proposed block diagram is show in the figure. This project consists of FPGA Controller kit and interfacing, GSM/GPRS module, GPS module, android Apps. This controller used to collection of GPS data and pelt (run very quickly) the LCD display. GPS module is used to send the person tracking data's to monitoring person, it is find out the accurate (current) location.

Figure : *FPGA Controller*

In the FPGA controller contained Person tracking activities (such as (1) Go to worship god.(2).Go to Park.(3).Go to relatives house.(4). Go to cinema and e.t.c.,) are programmed by using Hardware designed in FPGA system using Verilog/VHDL code. . Xilinx software is mostly easy development tool for FPGA Core applications. This module is implemented in VHDL/Verilog coding

LCD Display unit is shows the longitudes and latitude values (of GPS) of a person, and GSM/GPRS sends sms text alert message automatically to monitor person (parent). Receiver can monitor in android apps mobile / computer. If a person becomes important to provide a security and contact someone in case of emergency. Device can be programmed in such a way that, it one touch dial button (SOS) will send alert message and call to monitor parson, and they lift call and listen what they said and surroundings actions is going on. In case of emergency and you can reach to help your loved once.

(NSK GPS with RS 232) GPS and (SIM300)GSM is a compact device integrated with internal Battery, Small size, long lifetime, mobility and universal configuration of the device ensures wide spectrum of its application from people tracking, track control to special or secret tasks. GeoFence Function allow to set restricted geographical areas and devices will send warning messages whenever the object crosses the zone.

Android APPS

Android mobile phone is very popular in this world. Eclipse software is used for Creating new app. Person tracking app is installed in your mobile (android apps will be installed in android os). Google map shows the information about the person's location & street and total information. At the same time the person's data are updated to the monitoring person (parent), all information is automatically collected via URL (GPRS).Android apps developed by java (j2mobile edition) language.

GPS modem

GPS USAGES: Localization, Tracking, Maps,Time measurement

Each GPS satellite transmits radio signals that enable the GPS receivers to calculate where it's location on the Earth and convert the calculations into geodetic **latitude**, **longitude** and velocity. A receiver needs signals from at least three GPS satellites to pinpoint your position.

GPS Receivers commonly used in most tracking systems can only receive data from GPS Satellites. They cannot communicate back with GPS or any other satellite. A system based on GPS can only calculate its location but cannot send it to central control room.

GSM modem

(NSK GPS with RS 232) GPS and (SIM300) GSM the GSM Modem supports popular "**AT**" command set so that users can develop applications quickly. The GSM module is interfacing with FPGA and implemented by using AT commands to initiate and send the information (message) to Mobile phones.

Figure: GPS modem

Figure: GPS modem

This data also send to the control room & parent via SMS/call. In android mobile displays the latitude, longitude value and address of current location (point out the current location in the gmap). GSM Modem provides full functional capability to Serial devices to send SMS and Data over GSM Network. If press the sos button automatically call go to **control Room** or **corresponding parent** number .They lift call and listen what is happening surrounding of your loved one and Control room every one 10 min's once taken for backup's so you protect your child from incidents 'and know information about condition of your loved once. Real time implementation is very effectively in this project. Android apps another implementation it inform itself (text to speech).

Hardware requirement

1. FPGA controller kit
2. GPRS/GSM module (sending and receiving the data)
3. GPS module (find out location)
4. Display unit (LCD display shows lati,long values of gps)
5. Android apps mobile phone (for showing-map and monitoring)
6. DATA backup and monitoring purpose used for PC.

Software's used in Application

* android SDK packages(4.0) (Eclipse Helios)
* XILINX ISE 12.1i version(writing for VHDL/Verilog code)
* emulator (android apps checking simulation)

Applications include

* Parents use it as a child tracker or child locator
* Families monitor loved ones, particularly those who wander, such as people with dementia, Down's syndrome or people who sleepwalk
* People who venture into remote locations, eg. horse riders, cyclists, canoeists, runners,
* motorcyclists or bird watchers may be monitored to ensure their safety
* Affordably protect your car, horse box or boat from theft. even if there's no electricity (use a solar panel)
* Provide peace of mind to kids by letting them know where their parents are Find your miss-ing phone
* Vulnerable people who want a panic but-ton that will allow help to find them

Conclusion

A New generation automatic tracking and monitoring a person is very helpful to us.The main intention is person activities are programmed in FPGA core, it is always interfacing with GPS and GPRS/GSM module, if a person arrives in desired location it automatically send a SMS to the receiver as well represented the current address of location in a g-map by using AndroidApps. It also provides security and ability to contact our dear one in case of emergency. Device can be programmed in such a way that, it's one touch dial SOS button will send you alerts and call you in case of emergency and you can help your loved once and if person is avoid the desired track automatically give alarm to monitor person for quick alert and also send message of its exact location. When monitor person easy to know about their loved once and take action in time so that over come from danger. This project gives indirectly known information.

Output demo

Distance Analysis and Secure Smart Banking Using Central FPGA

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ABSTRACT

Abstract - Automated teller machines (ATMs) are well known devices typically used by individuals to carry out a variety of personal and business financial transactions and/or banking functions. ATMs have become very popular with the general public for their availability and general user friendliness. ATMs are now found in many locations having a regular or high volume of consumer traffic. For example, ATMs are typically found in restaurants, supermarkets, Convenience stores, malls, schools, gas stations, hotels, work locations, banking centers, airports, entertainment establishments, transportation facilities and a myriad of other locations. This has added new capabilities and features, however, most of the time, the implementations are proprietary and networking is not always possible. Yet there is an increasing demand for smart banking, where appliances react automatically to changing environmental conditions and can be easily controlled through one common device. This paper presents a possible solution whereby the user controls devices by employing a central Field Programmable Gate Array (FPGA) controller to which the devices and sensors are interfaced. Control is communicated to the FPGA from a mobile phone through its GSM interface. ATMs are typically available to consumers on a continuous basis such that consumers have the ability to carryout their ATM financial transactions and/or banking functions at any time of the day and on any day of the week.

Keywords

ATM terminal; face recognition; image enhancement; GSM MODEM.

INTRODUCTION

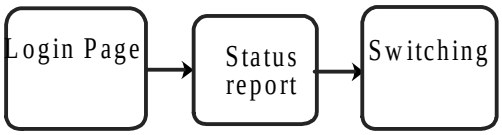
A automated teller machine (ATM) or the automatic banking machine (ABM) is a computerized telecommunications device that provides theclients of a financial institution with access to financial transactions in a public space without the need for a cashier, human clerk or bank teller. On most modern ATMs, the customer is identified by inserting a plastic ATM card with a magnetic stripe or a plastic smartcard with a chip, that contains a unique card number and some security information such as an expiration date . Authentication is provided by the customer entering a personal identification number (PIN).

Using an ATM, customers can access their bank accounts in order to make cash withdrawals (or credit card cash advances) and check their account balances as well as purchase cell phone prepaid credit. If the currency being withdrawn from the ATM is different from that which the bank account is denominated. Thus, ATMs often provide the best possible exchange rate for foreign travelers and are heavily used for this purpose as well.

ATMs are known by various other names including Automated Transaction Machine, automated banking machine, cash point (in Britain), money machine, bank machine, cash machine, hole-in-the-wall, Banc mat (in various countries in Europe and Russia), Multibank (after a registered trade mark, in Portugal), and Any Time Money (in India).

II. THE CHARACTERISTICS OF THE SYSTEM DESIGN

Mobile Section:



Automated functions through image processing Transaction based on subscriber identity module Security maintenance by behavior recognition Effective mobile communication for entire process Alert module for preventing illicit transactions Each process intimated by voice annunciation module Mobile scanning device scans SIM number through GSM Modem Which data given to the Teller machine for further processing At the same time, web camera captures the images and comparing using digital signal processing If images and PIN number are same then further processing continued Otherwise it gives alarm through Alert module Each processing information produces by

III. HARDWARE DESIGN AND SOFTWARE DESIGN

The design of entire system consisted of two part which are hardware and software. The hardware are designed by the rules of embedded system, and the steps of software consisted of three parts. The more details are shown as follows.

A. Hardware Design

Before using the ATM terminal, the client's feature will be connected to the remote face detection image datas-erver to match face detection image data with the master's, if the result isn't correct, the system will call police automatically and send alarm to the credit card owner. The block diagram of hardware design is shown in figure1.

B. Software design

The design was component of three parts included the design of main program flow chart, the initializing ones, and the algorithm of face detection recognition flow chart.

This system of software is implemented by the steps as follows: first of all, the Linux kernel and the File system are loaded into the main chip. The next, the system is initialized to implement specific task, such as checking ATM system, GSM communication and so on, and then each module reset for ready to run commands. Before using ATM terminal, the mobile number and face detection of the customer is required.

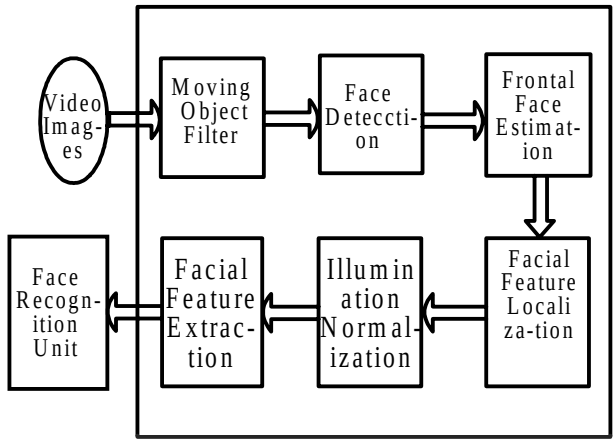


Figure 2 : *Flow diagram for face detection*

First the system is required the owner's face detection. If all the recognition is right, the system would send password to the Account holder and he will enter the same password in touch screen for accessing the ATM Terminal. If Authentication Failure then it send the alert message to the Account holder and Bank. The overall flow chart of software is shown in

In the process of inputting face detection, the implement which is a linear sensor that captures face detection images by sweeping the face over the sensing area, will used for acquiring the image of face detection. This product embed true hardware based 8- way navigation and click functions. The face detection information will be temporarily stored in SRAM and upload to the remote image data server to compare through bank network. The result of process will fpga. to the Account holder and he will enter the same password in touch screen for accessing the ATM Terminal. If Authentication Failure then it send the alert message to the Account holder and Bank. The overall flow chart of software is shown in 3.

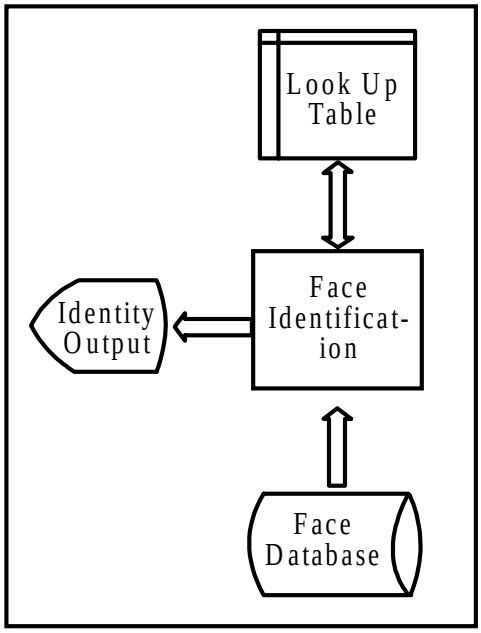


Figure 3 : *The flow chart of Face Detection Unit*

The initializing process means that set the hardware and software and then start the multiple mission module, each module will be started according to the priority processes. At first, initialize the system clock, and execute the codes of open interrupt and the open interrupt task. Then, the system would judge and enter process of module. finally, the system would start to attempt multiple tasks The initializing flow chart is shown in figure 3.

C. The design of face detection algorithm

The design of algorithm based on face detection is so vital for the whole system. We would approach two steps to process the images of fingerprint.

1) The detail of face detection process

The first step was the acquisition of face detection image by above device mentioned in the algorithm, and the results could be sent to the following process. secondly, pre-processing the images acquired. After obtain the face detection image, it must be pre-processing. Generally, pre-processing of one's is filtering, histogram computing, image enhancement and image binarization. Lastly, the characteristic value was extracted, and the results of the above measures would be compared with the information of owner's face detection in the database so as to verify whether the character is matched, and then the system returned the results matched or not.

2) The design of face detection image enhancement

Face detection module is an extremely important part of the system, the high-quality images was the major factors of influencing the performance in the system. The algorithm of face detection based on the algorithm of Gabor and direction filter was used. Face detection enhancement algorithm based on Gabor filter could be better to remove noise, strengthen the definition between the ridge and valley, it could significantly improve the image enhancement processing capacity, but this algorithm was slow in dealing with the high capacity requirements.

GSM

Global System for Mobile Communications (GSM: originally from Group Special Mobile) is the most popular standard for mobile phones in the world. Its promoter, the GSM Association, estimates that 82% of the global mobile market uses the standard GSM is used by over 2 billion people across more than 212 countries and territories. GSM differs from its predecessors in that both signalling and speech channels are digital call quality, and thus is considered a second generation (2G) mobile phone system. This has also meant that data communication was built into the system using the 3rd Generation Partnership Project (3GPP). GSM also pioneered a low-cost alternative to voice calls, the Short message service. GSM is a digital mobile telephone system that is widely used in Europe and other parts of the world.

GSM uses a variation of Time Division Multiple Access(TDMA) and GSM is the most widely used of the three digital wireless telephone technologies (TDMA, GSM, and CDMA). GSM digitizers and compresses data, then sends it down a channel with two other streams of user data, each in its own time slot. It operates at either the 900 MHz or 1,800 MHz frequency band. GSM is the de facto wireless telephone standard in Europe. GSM has over one billion users worldwide and is available in 190 countries.

Technical details

GSM is a cellular network, which means that mobile phones connect to it by searching for cells in the immediate vicinity. GSM networks operate in four different frequency ranges.

Most GSM networks operate in the 900 MHz or 1800 MHz bands. Some countries in the Americans(including Canada and the United States) use the 850 MHz and 1900 MHz bands because the 900 and 1800 MHz frequency bands were already allocated. The rarer 400 and 450 MHz

frequency bands are assigned in some countries, notably Scandinavia, where these frequencies were previously used for first-generation systems.

The Future of GSM

GSM together with other technologies is part of an evolution of wireless mobile telecommunication that includes High-Speed Circuit-Switched Data(DSCSD), General Packet Radio System (GPRS), Enhanced Data rate for GSM Evolution (EDGE), and Universal Mobile Telecommunications Service(UMTS).

CONCLUSIONS

The implement image-recognition techniques that can provide the important functions required by advanced intelligent ATM Security, to avoid theft and protect the usage of unauthenticated users**.** Secured and safety environment system for automobile users will be provided by implementing this project. We can predict the theft by using this system in our day to day life.

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Built - in Self Testing of High Performance and Low Power VLSI Circuits Using Accumulator Based 3 - Weight Pattern Generation

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ABSTRACT

High performance, Low hardware overhead and fault coverage of a circuit vital problem in Very Large Scale Integrated circuits and systems. To overcor this problem Pseudorandom Built-in Self Testing (BIST) generation schemes have been used in Integrated Circuits mostly. Generally Pseudorandom Pattern Generators (PRPG) is used for generating test patterns (TPG).In the proposed system Weighted Pseudorandom BIST methods have been utilized in order to minimize the number of test vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1 and 0.5 have been successfully utilized so for, for test pattern generation. Since, they result in both low consumed power and low testing time with high performance of the circuits. The proposed method generates a set of patterns with three weights 0, 0.5, and 1 using accumulator. Accumulators based on addition or subtraction can be used as test pattern generators, since these are commonly available in every current VLSI chips. This method can be efficiently utilized to drive down the hardware of BIST pattern generation as well. Automatic Test Pattern Generation (ATPG) generates the pseudorandom vectors for a benchmark circuits by using 3-weight pattern generators. Thus, in the proposed method number of test vectors are minimized with maximum fault coverage.

Key words : *VLSI testing, Built-in self-test (BIST), Circuit Under Test (CUT), Test Vectors (TV), Weighted test pattern generation.*

I. INTRODUCTON

Advances in VLSI technology have led to the fabrication of chips that contain a very large number of transistors. The task of testing such a chip to verify correct functionality is extremely complex and often very time consuming. In addition to the problem of testing the chips themselves, the incorporation of the chips into systems has caused test generations cost to grow exponentially. A widely accepted approach to deal with the testing problem at the chip level is to incorporate Built-In-Self-Test (BIST) capability inside a chip. Built- In-Self-Test (BIST) is the capability of a circuit to test itself. BIST is a design technique in which parts of a circuit are used to test the circuit itself. BIST represents a merger of the concepts of built-in test (BIT) and self- test. This increases the controllability and the observability of the chip, thereby making the test generation and fault detection easier. The test patterns and the expected responses of the circuit under test (CUT) to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses match the expected ones. Ideally, a BIST scheme should be easy to implement and must provide high fault coverage. Pseudorandom built-in self-test (BIST) generators have been widely utilized to test integrated circuits and systems. The arsenal of pseudorandom generators includes, among others, linear feedback shift registers (LFSRs) [1], cellular automata [2], and accumulators driven by a constant value [3]. For circuits with hard-to-detect faults, a large number of random patterns have to be generated before high fault coverage is achieved. Therefore, weighted pseudorandom techniques have been proposed where inputs are biased by changing the probability of a'0' or a '1' on a given input from 0.5 (for pure pseudorandom tests) to some other value [10], [15].

Weighted random pattern generation methods relying on a single weight assignment usually fail to achieve complete fault coverage using a reasonable number of test patterns since, although the weights are computed to be suitable for most faults, some faults may require long test sequences to be detected with these weight assignments if they do not match their activation and propagation

requirements. Multiple weight assignments have been suggested for the case that different faults require different biases of the input combinations applied to the circuit, to ensure that a relatively small number of patterns can detect all faults [4]. Approaches to derive weight assignments for given deterministic tests are attractive since they have the potential to allow complete coverage with a significantly smaller number of test patterns [10]. In order to minimize the hardware implementation cost, other schemes based on multiple weight assignments utilized weights 0, 1, and 0.5. This approach boils down to keeping some outputs of the generator steady (to either 0 or 1) and letting the remaining outputs change values (pseudo-) randomly (weight 0.5). This approach, apart from reducing the hardware overhead has beneficial effect on the consumed power, since some of the circuit under test (CUT) inputs (those having weight 0 or 1) remain steady during the specific test session [30]. Pomeranz and Reddy [5] proposed a 3-weight pattern generation scheme relying on weights 0, 1, and 0.5. The choice of weights 0, 1, and 0.5 was done in order to minimize the hardware implementation cost. Wang [8], [13] proposed a 3-weight random pattern generator based on scan chains utilizing weights 0, 1, and 0.5, in a way similar to [5]. Recently, Zhang *et al.* [9] renovated the interest in the 3-weight pattern generation schemes, proposing an efficient compaction scheme for the 3- weight patterns 0, 1, and 0.5. From the above we can conclude that 3-weight pattern generation based\ on weights 0, 1, and 0.5 has practical interest since it combines low implementation cost with low test time. Current VLSI circuits, e.g., data path architectures, or digital signal processing chips commonly contain arithmetic modules [accumulators or arithmetic logic units (ALUs)]. This has fired the idea of Arithmetic BIST (ABIST) [6]. The basic idea of ABIST is to utilize accumulators for built-in testing (compression of the CUT responses, or generation of test patterns) and has been shown to result in low hardware overhead and low impact on the circuit normal operating speed [22]– [27]. In [22], Munich *et al.* presented an accumulator- based test pattern generation scheme that compares favorably to previously proposed schemes.

In [7], it was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have acceptable pseudorandom characteristics, if the input pattern is properly selected. However, modules containing hard- to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns [24], [25]. In order to overcome this problem, an accumulator- based weighted pattern generation scheme was proposed in [11]. The scheme generates test patterns having one of three weights, namely 0, 1, and 0.5 therefore it can be utilized to drastically reduce the test application time in accumulator- based test pattern generation. However, the scheme proposed in [11] possesses three major drawbacks: 1) it can be utilized only in the case that the adder of the accumulator is a ripple carry adder; 2) it requires redesigning the accumulator; this modification, apart from being costly, requires redesign of the core of the data path, a practice that is generally discouraged in current BIST schemes; and 3) it increases delay, since it affects the normal operating speed of the adder.

In this paper, a novel scheme for accumulator-based 3-weight generation is presented. The proposed scheme copes with the inherent drawbacks of the scheme proposed in [11]. More precisely: 1) it does not impose any requirements about the design of the adder (i.e., it can be implemented using any adder design); 2) it does not require any modification of the adder; and hence, 3) does not affect the operating speed of the adder. Furthermore, the proposed scheme compares favorably to the scheme proposed in [11] and [22] in terms of the required hardware overhead.

This paper is organized as follows. In Section II, the idea underlying the accumulator-based 3-weight generation is presented. In Section III, the design methodology to generate the 3-weight patterns utilizing an accumulator is presented. In Section IV, the proposed scheme is compared to the previously proposed ones. Finally, Section V concludes this paper.

II. ACCUMULATOR-BASED 3-WEIGHT PATTERN GENERATION

We shall illustrate the idea of an accumulator- based 3-weight pattern generation by means of an example. Let us consider the test set for the c17 ISCAS benchmark [12], [31] given in Table I.

Test vector	Inputs A[4:0]
T1	00101
T2	01010
T3	10010
T4	11111

TABLE II

TRUTH TABLE OF THE FULL ADDER

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	0	0	1	1	0	$C_{out} = C_{in}$
3	0	1	0	1	0	$C_{out} = C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	1	0	1	0	1	$C_{out} = C_{in}$
7	1	1	0	0	1	$C_{out} = C_{in}$
8	1	1	1	1	1	

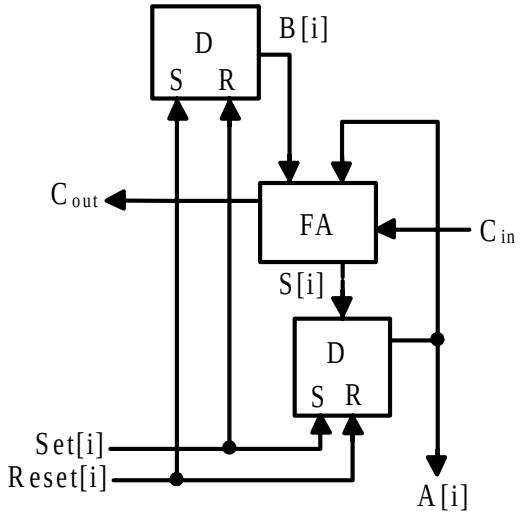

Fig.1: *Accumulator Cell*

Starting from this deterministic test set, in order to apply the 3-weight pattern generation scheme, one of the schemes proposed in [5], [8], and [9] can be utilized. According to these schemes, a typical weight assignment procedure would involve separating the test set into two subsets, S1 and S2 as follows: S1= {T1, T4} and S2= {T2, T3}. The weight assignments for these subsets is W (S1)= {-,-,1,-,1} and W (S2)= {-,-,0,1,0} where a "-" denotes a weight assignment of 0.5, a "1" indicates that the input is constantly driven by the logic "1" value, and "0" indicates that the input is driven by the logic "0" value. In the first assignment, inputs A[2] and A[0] are constantly driven by "1", while inputs A[4], A[3], A[1] are pseudo randomly generated (i.e., have weights 0.5). Similarly, in the second weight assignment (subset S2), inputs A[2] and A[0] are constantly driven by "0", input A[1] is driven by "1" and inputs A[4] and A[3] are pseudo randomly generated.

The above reasoning calls for a configuration of the accumulator, where the following conditions are met: 1) an accumulator output can be constantly driven by "1" or "0" and 2) an accumulator cell with its output constantly driven to "1" or "0" allows the carry input of the stage to transfer to its carry output unchanged. This latter condition is required in order to effectively generate pseudorandom patterns in the accumulator outputs whose weight assignment is "-".

III. DESIGN METHODOLOGY

The implementation of the weighted-pattern generation scheme is based on the full adder truth table, presented in Table II. From Table II we can see that in lines #2, #3, #6, and #7 of the truth table, C_{OUT} = CIN . Therefore, in order to transfer the carry input to the carry output, it is enough to set A[i]= NOT(B[i]). The proposed scheme is based on this observation.

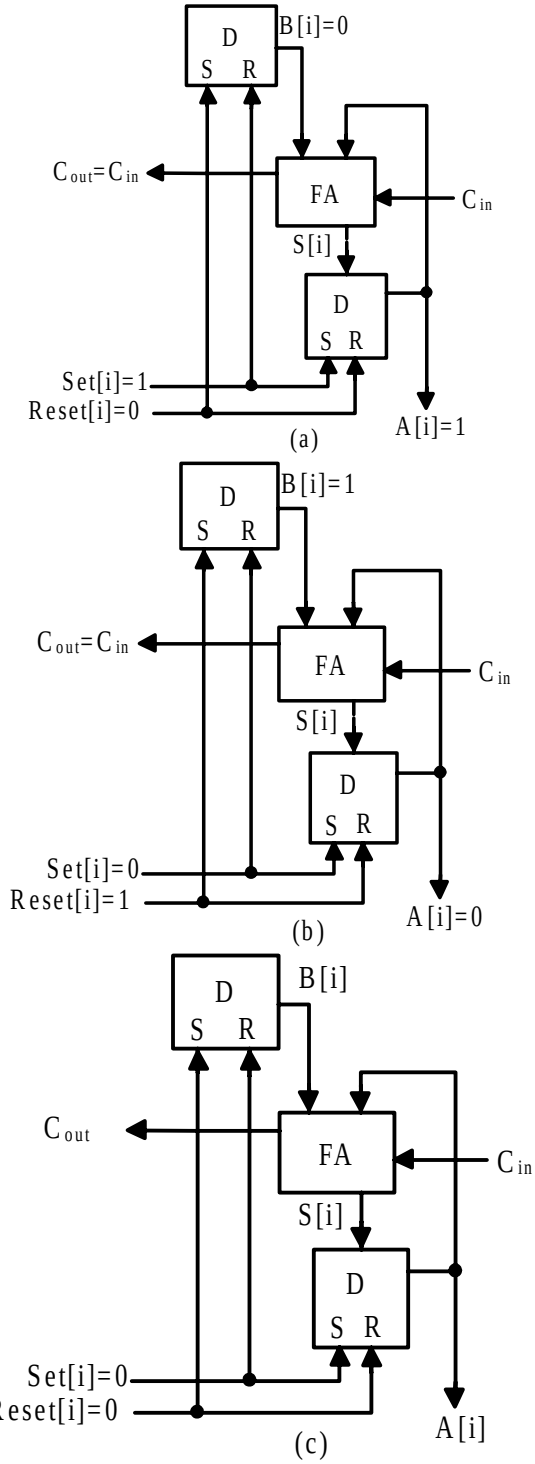

Fig.2: *Configurations of the accumulator cell of Fig.1*

In Fig. 2(a) we present the configuration that drives the CUT inputs when A[i] = 1 is required. Set[i] =1 and Reset[i] = 0 and hence A[i] = 1 and B[i] = 0 . Then the output is equal to 1, and C_{IN} is transferred to C_{OUT}

In Fig. 2(b), we present the configuration that drives the CUT inputs when A[i] = 0 is required. Set[i]=0 and Reset[i]=1 and hence A[i]=0 and B[i]=1.

Then, the output is equal to 0 and C_{IN} is transferred to C_{OUT}.

In Fig. 2(c), we present the configuration that drives the CUT inputs when A[i] = "-" is required. Set[i]=0 and Reset[i]=0 . The D input of the flip-flop of register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate satisfactorily random patterns to the inputs of the CUT.

In Fig. 3, the general configuration of the proposed scheme is presented. The Logic module provides the Set[n-1:0] and Reset[n-1:0] signals that drive the S and R inputs of the Register A and Register B inputs. Note that the signals that drive the S inputs of the flip-flops of Register A, also drive the R inputs of the flip-flops of Register B and vice versa.

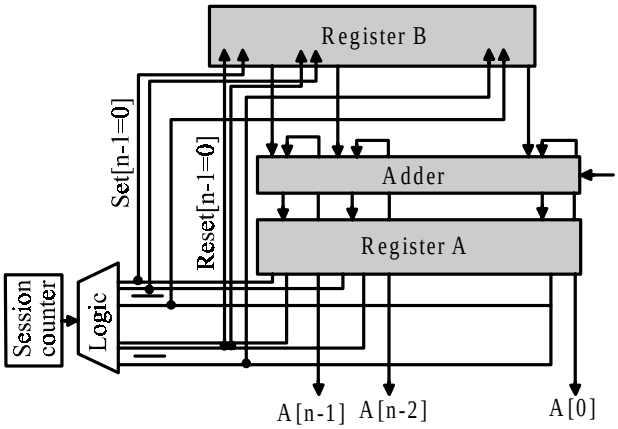

Fig.3: *Proposed Scheme*

The implementation of the proposed weighted pattern generation scheme is based on the accumulator cell presented in Fig. 1, which consists of a Full Adder (FA) cell and a D-type flip-flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs. In Fig. 1, we assume, without loss of generality, that the set and reset are active high signals. In the same figure the respective cell of the driving register B[i] is also shown. For this accumulator cell, one out of three configurations can be utilized, as shown in Fig. 2

IV. COMPARISONS

In this section, we shall perform comparisons in three directions. In Section IV-A, we shall compare the proposed scheme with the accumulator based 3-weight generation scheme that has been proposed in [11]. In Section IV-B, we shall compare the proposed scheme with the 3-weight scan schemes that have been proposed in [5] and [8]. In Section IV-C, in order to demonstrate the applicability of the proposed scheme we shall compare the proposed scheme with the accumulator- based test pattern generation scheme proposed in [22].

A. Comparisons with [11]

The number of test patterns applied by [11] and the proposed scheme is the same, since the test application algorithms that have been invented and applied by previous researchers, e.g., [5], [8], [9] can be equally well applied with both implementations. Therefore, the comparison will be performed with respect to: 1) the hardware overhead and 2) the impact on the timing characteristics of the adder of the accumulator.

Both schemes require a session counter in order to alter among the different weight sessions; the session counter consists of $\log_2 k$ bits where k is the number of test sessions (i.e., weight assignments) of the weighted test set. The scheme proposed in [11] requires the redesign of the adder; more precisely, two NAND gates are inserted in each cell of the ripple-carry adder. In order to provide the inputs to the set and reset inputs of the flip flops, decoding logic is implemented, similar to that in [8]. For the proposed scheme, no modification is imposed on the adder of the accumulator. Therefore, there is no impact on the data path timing characteristics. In Table III we present comparison results for some of the ISCAS'85 benchmarks. In the first column of Table III, we present the benchmark name; in the second and third columns we present the hardware overhead of the accumulator-based scheme proposed in [11] and in this work, respectively; in the fourth column we present the decrease of the proposed scheme over [11]. In the fifth through the seventh columns, we present the delay of the adder in terms of number of gates that the carry signal has to traverse, from the CIN input of the adder (lower stage full adder cell) to the C_{OUT} output (higher stage full adder cell), as well as the respective decrease obtained by the proposed scheme.

Circuit	Hardware overhead			Delay from C_{in} to C_{out}				
				(Ripple)			(prefix)	
Name	[11]	Pr Op.	de cr.	[11]	pr op.	de .cr.	pr op	de cr.
c8080	41%	8%	81%	240	180		24	90%
c1355	28%	7%	74%	164	123		22	87%
c1908	13%	3%	77%	132	99		21	84%
c2670	34%	8%	75%	932	699	20%	32	97%
c3540	11%	5%	57%	200	150		23	89%
c5315	17%	2%	90%	712	534		30	96%
c7552	17%	4%	75%	828	621		31	96%

TABLE III COMPARISONS WITH [11]

In Table III, the hardware overheads are calculated in gate equivalents, where an n-input NAND or NOR accounts for 0.5 _ gates and an inverter accounts for 0.5 gates, as proposed in [8]. For the calculation of the delay in the adder operation (columns under heading $-\#\text{gates from } C_{IN} \text{ to } C_{OUT} -$)we have considered both

ripple carry and prefix adder implementations. For the comparisons of the ripple carry adder implementations, the adder cell utilized in [11] is considered; in the cell presented in [11], initially the delay from the C_{IN} to C_{OUT} of the adder *cell* is two NAND gates and one XOR gate; in the modified cell proposed in [11], the delay is increased to three NAND and one XOR gate; we have considered that the delay of a NAND gate is one gate equivalent, while the delay of an XOR gate is two gate equivalents. Since the implementation of the proposed scheme does not rely on a specific adder design, the utilization of a prefix adder can result in impressive results. For the calculation of the delay of prefix adders, the formula obtained by [29] is utilized, where the delay is of the order $4 * \log_2 n$, where _ is the number of the adder stages. From Table III, we can see that the proposed scheme results in 57%–90% decrease in hardware overhead, while at the same time achieving a decrease in operational delay overhead that ranges from 84% to 97% for the considered benchmarks.

B. Comparisons with Scan-Based Schemes [5], [8]

Since the test application algorithms that have been invented and applied by [5], [8], and [9] can be equally well applied with the proposed scheme, test application time is similar to that reported there. Therefore, the comparison will be performed with respect to hardware overhead. In the 3-weight pattern generation scheme proposed by Pomeranz and Reddy in [5] the scan chain is driven by the output of a linear feedback shift register (LFSR). Logic is inserted between the scan chain and the CUT inputs to fix the outputs to the required weight (0, 0.5, or 1). In order to implement the scheme [5], a scan-structure is assumed. Furthermore, an LFSR required to feed the pseudorandom inputs to the scan inputs is implemented (the number of LFSR stages is $\log_2 n$, where n is the number of scan cells), as well as a scan counter, common to all scan schemes. A number of 3-gate modules is required for every required weighted input (in [5, Table V], the hardware overhead is calculated for the ISCAS'85 benchmarks).

TABLE IV COMPARISONS WITH THE SCAN SCHEMES ROPOSED IN [5] and [8]: the LFSR implementation. In order to calculate the numbers in the second column, we utilized the data found in [5, Table V]. For the scheme in [8], the LFSR, the scan counter and the decoding logic are required; the hardware overhead for the decoding logic has been quoted from [8, Table I]

Cut	Pomeranz[5] Weighing gates + scan counter+ LFSR=Total				Wang [8] LFSR+ Decoding logic + Scan counter= Total				Proposed
c880	5	47	47	99	47	6	47	100	27
c1355	1	43	43	87	43	6	43	92	38
c1908	0	40	40	80	40	2	40	82	23
c2670	542	63	63	668	63	39	63	165	101
c3540	2	45	45	92	45	24	45	114	73
c5315	0	60	60	120	60	7	60	127	39
c7552	1134	62	62	1258	62	66	62	190	139

C. Comparisons with [22]

In [22], Munich *et al.* proposed a methodology to reduce the total test time using an accumulator-based scheme. The scheme operates in test sessions based on triplets of the form (S, I, L), where S is the starting value of the accumulator, I is the increment, and L is the number of cycles the increment is applied before going to the next session. For the comparisons we have utilized the data from [22, Table I], and have considered that the seeds are stored in a ROM; for the hardware calculation we have considered that a ROM bit is equivalent to ¼ gates, as has been also considered in [20] and [32]. The comparison data for some of the ISCAS'85 and ISCAS'89 benchmarks are presented in Table V, where the same fault coverage, i.e., 100% is targeted.

TABLE V COMPARISONS WITH THE SCHEME PROPOSED IN [22]:

Benchmark circuit	h/w	#inp	[22] tests	[22] h/w	proposed #tests	proposed h/w
c880	383	60	1112	36	768	27
c1355	546	41	1409	26	1024	38
c1908	880	33	3198	23	1536	23
c2670	1193	157	1962	1386	4096	101
c 3540	1669	50	2167	31	1536	73
c5315	2307	178	1453	189	2048	39
c7552	3512	206	2018	1090	4608	139
c5378	1004	214	2078	791	5120	47
s9234	2027	247	14803	4763	11264	181
S13207	2573	700	14476	7497	12288	61
s15850	3448	611	14902	18438	21504	159
s38584	11448	1464	8449	26235	16384	82
Average values			5744	5042	6848	81

Wang [8] proposed a low-overhead 3-weight random BIST scheme, again based on scan chains. He proposed two schemes, namely *serial fixing BIST* and *parallel fixing BIST*. Serial fixing scheme is shown to be more costly [8]; therefore we shall concentrate our comparisons to the parallel fixing BIST scheme. For an n-input CUT and, assuming the availability of the scan chain, the hardware overhead, apart from the LFSR to generate the pseudorandom inputs and the scan counter, includes a *decoding logic*. The hardware overhead of the decoding logic for some of the ISCAS benchmarks is calculated in [8, Table I]. All schemes require the application of the

session counter, required to alter among the different weight sessions. Schemes proposed in [5] and [8] are test per scan schemes, and, of course, assume the existence of scan capability of the latches of the design.

In Table IV, we have presented arithmetic results for some of the ISCAS'85 benchmarks. For the calculations in Table IV, we have assumed that schemes [5] and [8] are applied to a circuit with scan capability; therefore, the hardware overhead to transform the latches into scan latches is not taken into account. For the scheme proposed in [5], the total hardware overhead comprises the hardware for the weighting gates (second column), the scan counter and

In Table V, in the first three columns we present the benchmark characteristics (name, hardware overhead in gates and number of inputs). In the two columns to follow, we present the number of tests required for the scheme in [22], and the respective hardware overhead in gate equivalents. Next, we present the number of test patterns and hardware overhead for the proposed scheme. From Table V it is trivial to see that the proposed scheme presents an important decrease in the hardware overhead, while the number of tests is comparable, while in some cases it also outperforms the scheme in [22]. It is interesting to note that the hardware overhead (with respect to the hardware overhead of the benchmarks) is practical, in contrast to [22] which sometimes exceeds the benchmark hardware (c2670, s5378, s9234, s13207,s15850, s38584). It is also interesting to note the average values presented in the last line of the Table. The average increase in the number of tests is 19%, while the average decrease in hardware overhead is 98%.

V. CONCLUSION

Weighted pseudorandom BIST schemes have been efficiently utilized in order to drive down the number of vectors to achieve complete fault coverage in Built in Self Test (BIST) applications. Sets of patterns comprising weights 0, 0.5 and 1 have been successfully utilized within the weighted pattern generation paradigm. We have presented a user controllable, low hardware overhead accumulator-based 3-weight (0, 0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns without altering the structure of the adder. Comparisons with a previously proposed accumulator-based 3 weight pattern generation technique [11] indicate that the hardware overhead of the proposed scheme is lower (75%), while at the same time no redesign of the accumulator is imposed, thus resulting in reduction of 20%–95% in test application time. Comparisons with scan based schemes [5], [8] show that the proposed schemes results in lower hardware overhead. Finally, comparisons with the accumulator-based scheme proposed in [22] reveal that the proposed scheme results in significant decrease (98%) in hardware overhead.

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High Speed Memory Characterization Method for Transmitter and Receiver Parts of Processors

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ABSTRACT

Today's microprocessors have need to operate at very high IO speed to cater ti ever increasing computation need, so characterizing these IO's in a quick efficient and accurate manner is needed for us. The paper involves studying Transmitter (T_x^{er}) *and Receiver* (R_x^{er}) *blocks of memory interface of CPU and develop methods to characterized these IO's, suitable feedback to design is provided after analyzing the data and receiving with design. In this paper involves some analog analysis and design. Here it needs some software tool to implementation. This paper implements new method to increase the speed of the IO operations of the memory interface of CPU. This contain the usage of the NIDAQ6008 and analog design and the circuit design concepts and here it deals with the calculation of the R term, Pull-up, Pull-down resistors and Jitter and the de-embedding of the signal loss.*

I. INTRODUCTION

The semiconductor technology is growing in a faster rate in the world this is due to the Moore's law. The major thing in this is many issues due to uncertainties they may be the speed, area and may be the IO issues. To speed up the mechanism generally we prefer parallel technique. Here the main use of this paper is to increase the performance and reduce the cost of the setup.

This paper is used to enhance the design for the IO analysis of the memory interface of the CPU and develop the high speed IO characterization methods. Actually here we are to design the new setup the will reduce the cost around some dollars. And as per the time it will reduce by a factor of $1/8^{th}$ means the speed is increase by a factor of 8 of the previous speed.

II. LITERATURESURVEY

This paper is about how advantage it is when compare to the older version. And this is increase the speed of the IO operation and save the money in order of thousand dollars and save time to IO operation. Previous they are supposed to use the serial data acquisition devices but now we are implemented parallel data acquisition methodology to reach our requirements.

This survey indicates how this paper is appropriate to increase the performance with respect to the cost and speed from the below graphs. The variation in the time spent and the cost is given in the different plots as below

Number of switches and pins	Total cost in $k	The time after the parallel technique (estimated)	Time before parallel technique	Total cost in $k after parallel tech (estimated)
16	$32	1	16	$2
32	$64	2	32	$4
48	$96	3	48	$6
64	$128	4	64	$8
80	$160	5	80	$10
96	$192	6	96	$12

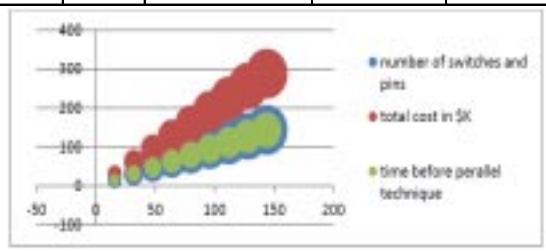

Figure1: *The plot of the cost and time with respect to switches and pins for older design.*

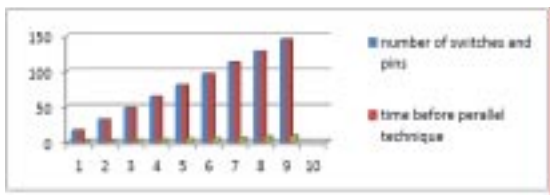

Figure2: *Comparison in terms of time.*

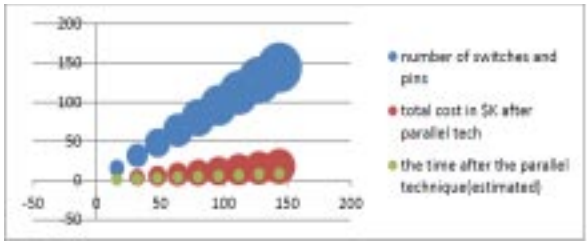

Figure3: *The plot of the cost and time with respect to switches and pins for new design (estimated)*

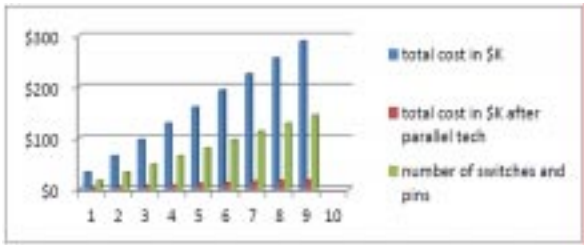

Figure4: *Comparison in terms of cost.*

III. NEWMETHODOLOGY

This is the block diagram of the new design. Here we are using the NI USB 6008 for the interface between the PC and the PCB of the constant current source design.

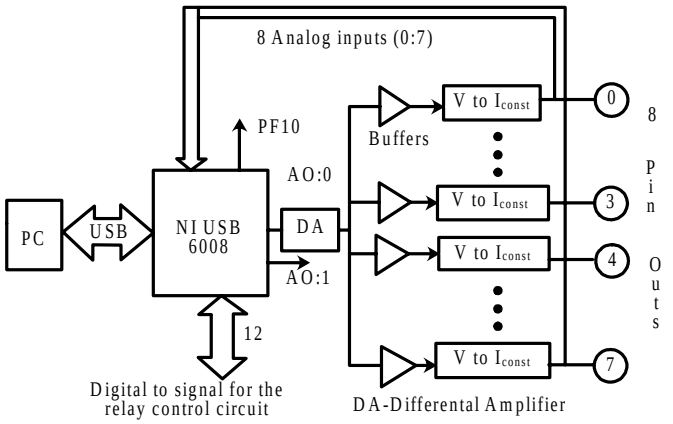

Figure5: *Block Diagram of New Design.*

Here we need to find out the ON Resistance of the pull up and pull down resister of the pin out which we are measuring the voltage across it by sending the constant current through it. After sending the constant current through the pin out then we can measure the output voltage from that point. Then we can store that value in the memory from the FIFO of the NI USB 6008. Here the main task is to design the constant bipolar current source which means based on the pin out condition. Internally it has a pull up and pull-down transistors. These transistors are ON once at a time based on the input that it exited. If the input is high then the pull down is going to be in ON condition and it offed the R of the ON transistor. And the current that is fed into that resister so our circuit acts as a current source. If the input is low then the pull up is going to be in ON condition and it offed the R_{up} of the ON transistor. And the current that is fed from that resister so our circuit acts as a current sink. The main parts of the design is

1. National Instruments USB-6008
2. Differential Amplifier(DA)
3. Constant current source's
4. Voltage follower
5. Relays

A. National Instruments USB-6008

The NI USB-6008 provides connection to eight single-ended analog input (AI) channels, two analog output (AO) channels, 12 digital input/output (DIO) channels, and a 32-bit counter with a full-speed USB interface.

Firmware

The firmware on the NI USB-6008 refreshes whenever the device is connected to a computer with NI-DAQmx. NI-DAQmx automatically uploads the compatible firmware version to the device. The firmware version may be upgraded when new versions of NI-DAQmx release.

The pin out of the NI USB-6008. Analog input signal names are listed as single-ended analog input name, AI x, and then differential analog input name, (AI x+/–).

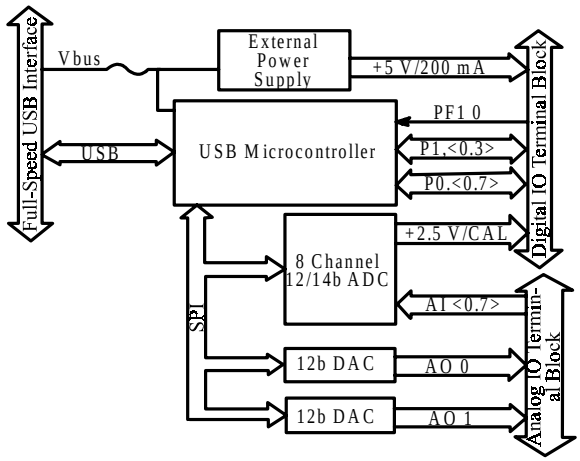

Figure6: *Block Diagram of NI USB-6008*

B. Bipolar Constant Current Source

Current source: An ideal current source, I, driving a resistor, R, and creating a voltage V. A **current source** is an electronic circuit that delivers or absorbs an electric current which is independent of the voltage across it. A current source is the dual of a voltage source. The term constant-current **sink** is sometimes used for sources fed from a negative voltage supply.

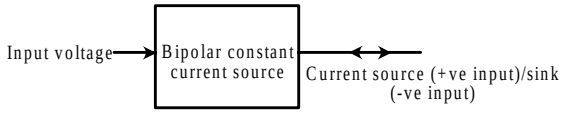

Figure7: *Bipolar Constant Current Source/Sink.*

Current sources and sinks are analysis formalisms which distinguish points, areas, or volumes through which current enters or exits a system. While current sources or sinks are abstract elements used for analysis, generally they have physical counterparts in real-world applications; e.g. the anode or cathode in a battery. In all cases, each of the opposing terms (source or sink) may refer to the same object, depending on the perspective of the observer and the sign conversion being used; there is no intrinsic difference between a source and a sink.

- A **source** is a flow of current into the load.
- A **sink** is a flow of current from the load.

The constant current is given by

$$"\text{Iout} = [(R2 + R3)/(R1 * R3)] * \text{Vdiff}"$$

IV. TOOLSUSING

The tools are Python and Multisim. Here python is used to develop the script and Multisim is used to simulate the analog circuits.

A. The Python Programming Language

The programming language you will learn is Python. Python is an example of a **high-level language**; other high-level languages you might have heard of are C, C++, Perl, and Java. There are also **low-level languages**, sometimes referred to as "machine languages" or "assembly Languages" Loosely speaking, computers can only run programs written in low-level languages.

Low-level languages are used only for a few specialized applications. Two kinds of programs process high-level languages into low-level languages: **interpreters** and **compilers**. An interpreter reads a high-level program and executes it, meaning that it does what the program says. It processes the program a little at a time, alternately reading lines and performing computations. A compiler reads the program and translates it completely before the program starts running. In this context, the high-level program is called the **source code**, and the translated program is called the **object code** or the **executable**. Once a program is compiled, you can execute it repeatedly without further translation. Alternatively, you can store code in a file and use the interpreter to execute the contents of the file, which is called a **script**. By convention, Python scripts have names that end with .py.

B. NI Multisim

NI Multisim (formerly MultiSIM) is an electronic schematic capture and simulation program which is part of a suite of circuit design programs, along with NI Ultiboard. Multisim is one of the few circuit design programs to employ the original Berkely SPICE based software simulation. Multisim was originally created by a company named Electronics Workbench, which is now a division of National Instruments. Multisim was originally called Electronics Workbench and created by a company called Interactive Image Technologies. At the time it was mainly used as an educational tool to teach electronics technician and electronics engineering programs in colleges and universities. National Instruments has maintained this educational legacy, with a specific version of Multisim with features developed for teaching electronics.

V. RESULTSANDFUTURESCOPE

* Complexity is reduced by replacing the Keithley switches by the new design.

* Speed of the operation is increased by a factor of 8.

* Cost is effective when compared to the older design.

In the second phase I am going to design and implement circuit diagram of my new design and the programing part. That is used to characterize the IO characteristics of the memory interface of CPU practically.

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Design of Vedic Multiplier for Digital Signal Processing Applications

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ABSTRACT

The speed of a multiplier is of utmost importance to any Digital Signal Process (DSPs). Along with the speed its precision also plays a major role. Although Floating point multipliers provide required precision they tend to consume more silicon area and are relatively slower compared to fixed point (Q-format) multipliers. In this paper we propose a method for fast fixed point signed multiplication based on Urdhava Tiryakbhyam method of Vedic mathematics. The coding is done for 16 bit (Q15) and 32 bit (Q31) fractional fixed point multiplications using Verilog and synthesized using Xilinx ISE version 12.2. Further the speed comparison of this multiplier with normal booth multiplier is presented. The results clearly indicate that Urdhava Tiryakbhyam can have a great impact on improving the speed of Digital Signal Processors.

Keywords

Q-format; Urdhava Tiryakbhyam; Vedic Mathematics; Fractional fixed point.

I. INTRODUCTION

Vedic Mathematics hails from the ancient Indian scriptures called “Vedas” or the source of knowledge. This system of computation covers all forms of mathematics, be it geometry, trigonometry or algebra. The striking feature of Vedic Mathematics is the coherence in its algorithms which are designed the way our mind naturally works. This makes it the easiest and fastest way to perform any mathematical calculation mentally. Vedic Mathematics is believed to be created around 1500 BC and was rediscovered between 1911 to 1918 by Sri Bharti Krishna Tirthaji (1884-1960) who was a Sanskrit scholar, mathematician and a philosopher [1]. He organized and classified the whole of Vedic Mathematics into 16 formulae or also called as sutras. These formulae form the backbone of Vedic mathematics. Great amount of research has been done all these years to implement algorithms of Vedic mathematics on digital processors. It has been observed that due to coherence and symmetry in these algorithms it can have a regular silicon layout and consume less area [2,3] along with lower power consumption. Normally signal processing algorithms are developed using high level languages like C or Mat lab using floating point number representations. The algorithm to architecture mapping using floating point number representation consumes more hardware which tends to be expensive. Fixed point number representation is a good option to implement at silicon level. Hence our focus in this work is to develop optimized hardware modules for multiplication operation which is one of the most frequently used operation in signal processing applications like Fourier transforms, FIR and IIR filters, image processing systems, seismic signal processing, optical signal processing etc. Any attempt to come out with an optimized architecture for this basic block is advantageous during the product development stages. Considering fixed point representation, 16 bit Q15 format and 32 bit Q31 format provide required precision for most of the digital signal processing applications and it is best suited for implementation on processors. The advantage it provides over floating point multipliers is in the fact that Q format fraction multiplications can be carried out using integer multipliers which are faster and consume less die area. DSP Processors like TMS320 series from Texas Instruments work on 16 bit Q15 format. In this paper we propose the implementation of fixed point Q-format [6] high speed multiplier using Urdhava Tiryakbhyam method of Vedic mathematics. Further we have also implemented multipliers using normal booth algorithm [8] and Xilinx parallel multiplier Intellectual Property and presented a comparative study on maximum frequency or speed of these multipliers.

The paper is organized into VI sections. Section II explains fixed point or Q-format representation of a number; III spreads light over Urdhava Tiryakbhyam method of Vedic mathematics; IV explains the architecture of proposed Q format Urdhava multipliers V presents the

results and comparison and lastly VI provides conclusion of the work.

II. FIXED POINT ARITHMETIC

An N-bit fixed point number [6] can be interpreted as either an integer or a fractional number. Integer fixed point is difficult to use in processors due to possible overflow. For e.g. In a 16-bit processor for signed integers the dynamic range is from -2^m to $2^{-15}-1$ -1 i.e. 32768 to 32767. If 500 is multiplied by 800 the result is 40000 which is an overflow. In order to overcome this situation fractional fixed point representation also known as Q-format is used.

A. Q-format Representation

In general any Q-format representation is denoted by Q*m.n*, where *m* is the number of bits to represent integer, *n* denotes number of bits to represent fractional part and the total number of bits is given by N = *m*+*n*+1 for signed numbers. For e.g. Q4.11 format signifies that a total of 16 bits are required to represent a fractional number in which 4 bits are reserved for the integer part and 11 bits for the fractional part and 1 bit indicates sign. Special cases of Q-format consist of zero bits to represent the integer part. Q0.15 (Q15) and Q0.31 (Q31) are two such formats for 16 bit and 32 bit representations respectively. As there is no integer part the fractional number has a range between 1 and -1. Therefore the products of such numbers also lie between 1 and -1. This property is best suited for implementing multipliers as the bit length of the product is same as the input bit length and thus Q-format finds its application in digital signal processing hardware.

An N-bit number in Q*m.n* format is represented as follows.[6]

$$a_{n+m}a_{n+m-1}.....a_n.a_{n-1}....a_1.a_0 \qquad .....(1)$$

Here the '.' between $a_n.a_{n-1}$ represents the fixed point and value of (1) is given by,

$$\left(a_{n+m}2^{N-1}+a_{n+m-1}2^{N-2}....+a_2 2^2+a_1 2+a_0\right)2^{-n}.$$

When we want to convert a fractional number in the range of the desired Q*m.n* format, we multiply it with 2^n. The resultant value is truncated or rounded off to the nearest integer. Therefore a small amount of precision loss is involved which reduces as the number of bits representing the fractional part increases. We prefer rounding technique since its error bias in both positive and negative direction is same [6]. Therefore the rounded value will be more precise. For e.g. Conversion of 0.2625 to Q15 format is done by multiplying it with 2^{15} which equals to 8601.6 which when rounded gives 8602. This is stored as 0010000110011010 in a 16 bit memory location. The most significant bit indicates sign of the number. If it is negative then 2's complement method is followed to store the number. Thus a fraction is converted to an integer in a Q-format and the choice of the decimal point lies entirely in the hands of the programmer.

In general a Q*m.n* format has a resolution of 2^{-n} and its dynamic range lies between $-2^m \;\; 2^m-2^n$. Therefore as the number of bits for fractional representation increases the resolution increases and as the number of bits for integer part increases the dynamic range increases. The resolution of Q15 format is 2^{-15}, and for Q31format it is 2^{-31}. Therefore a number represented in Q31 format has higher resolution and is more precise than the one in Q15 format. In this paper we mainly concentrate on Q15 and Q31 formats since they are best suited for implementing multipliers for DSP applications.

B. Q-format Multiplication

When two Q15 numbers are multiplied their product is 32 bits long as illustrated in Fig. 1. The product has a redundant or extended sign bit. Since the product stored in memory should also be a Q15 number we left shift the product by one bit and the most significant 16 bits (including sign bit) is multiplication of two Q15 format numbers. The process remains same for Q31 format wherein after left shifting the product by one bit, the most significant 32 bits are stored in the memory. Therefore with Q-format, multiplications of two fractional numbers can be carried out by using integer multiplications. Integer multiplications consume less area and are faster compared to floating point multipliers which is the major advantage of Q format representation.

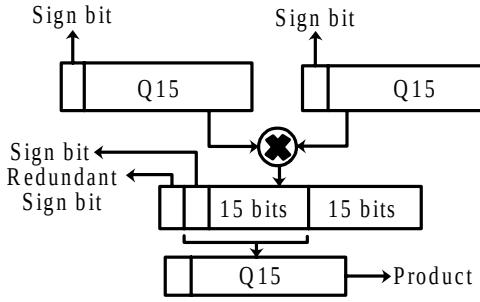

Figure. 1*. Multiplication of two Q15 format numbers yielding the product in Q15 format itself.*

III. URDHAVA TIRYAKBHYAM METHOD

Urdhava Tiryakbhyam [2] is a Sanskrit word which means vertically and crosswire in English. The method is a general multiplication formula applicable to all cases of multiplication. It is based on a novel concept through which all partial products are generated concurrently. Figure 2demonstrates a 4x4 binary multiplication using this method. The method can be generalized for any N x N bit

multiplicationThis type of multiplier is independent of the clock frequency of the processor because the partial products and their sums are calculated in parallel. The net advantage is that it reduces the need of microprocessors to operate at increasingly higher clock frequencies. As the operating frequency of a processor increases the number of switching instances also increases. This results in more power consumption and also dissipation in the form of heat which results in higher device operating temperatures. Another advantage of Urdhva Tiryakbhyam multiplier is its scalability. The processing power can easily be increased by increasing the input and output data bus widths since it has a regular structure [3]. Due to its regular structure, it can be easily layout in a silicon chip and also consumes optimum area [2]. As the number of input bits increase, gate delay and area increase very slowly as compared to other multipliers. Therefore Urdhava Tiryakbhyam multiplier is time, space and power efficient. The line diagram in figure. 2 illustrates the algorithm for multiplying two 4-bit binary numbers $a_2a_2a_1a_0$ and $b_3b_2b_1b_0$. The procedure is divided into 7 steps and each step generates partial products. Initially as shown in step 1

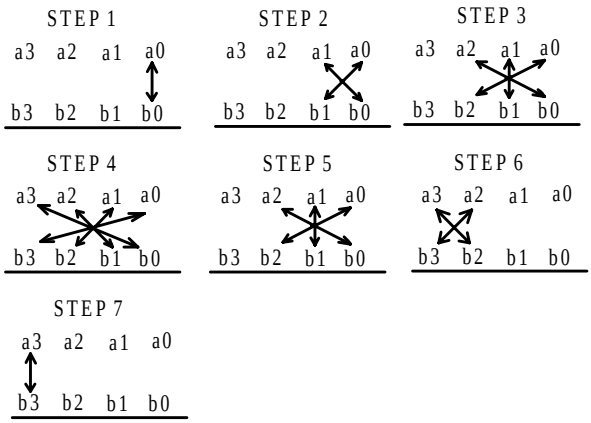

Figure. 2 *Multiplication of two 4 bit numbers using Urdhava Tiryakbhyam method.[7]*

of figure. 2, the least significant bit (LSB) of the multiplier is multiplied with least significant bit of the multiplicand (vertical multiplication). This result forms the LSB of the product. In step 2 next higher bit of the multiplier is multiplied with the LSB of the multiplicand and the LSB of the multiplier is multiplied with the next higher bit of the multiplicand (crosswire multiplication). These two partial products are added and the LSB of the sum is the next higher bit of the final product and the remaining bits are carried to the next step. For example, if in some intermediate step, we get the result as 1101, then 1 will act as the result bit(referred as rn) and 110 as the carry (referred as cn). Therefore cn may be a multi-bit number. Similarly other steps are carried out as indicated by the line diagram. The important feature is that all the partial products and their sums for every step can be calculated in parallel. Thus every step in fig. 2 has a corresponding expression as follows:

$$r0=a0b0. \quad (1)$$

$$c1r1=a1b0+a0b1. \quad (2)$$

$$c2r2=c1+a2b0+a1b1+a0b2. \quad (3)$$

$$c3r3=c2+a3b0+a2b1+a1b2+a0b3. \quad (4)$$

$$c4r4=c3+a3b1+a2b2+a1b3. \quad (5)$$

$$c5r5=c4+a3b2+a2b3. \quad (6)$$

$$c6r6=c5+a3b3. \quad (7)$$

With c6r6r5r4r3r2r1r0 being the final product [5].

Hence this is the general mathematical formula applicable to all cases of multiplication and its hardware architecture is shown in figure. 3.In order to multiply two 8-bit numbers using 4-bit multiplier we proceed as follows. Consider two 8 bit numbers denoted as AHAL and BHBL where AH and BH corresponds to the most significant 4 bits, AL and BL are the least significant 4 bits of an 8-bit number. When the numbers are multiplied

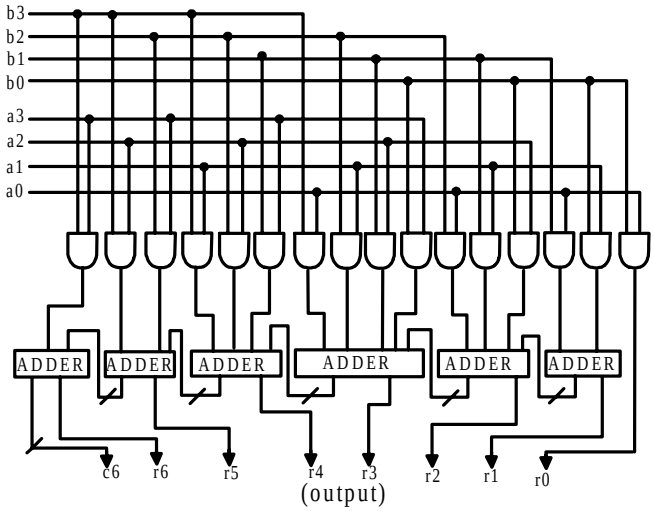

Figure. 3.*Hardware architecture of 4 X 4 Urdhva Tiryakbhyam multiplier. [5]*

according to Urdhava Tiryakbhyam (vertically and crosswire) method, we get,

AH AL

BH BL

_____

(AH x BH) + (AH x BL + BH x AL) + (AL x BL).

Thus we need four 4-bit multipliers and two adders to add the partial products and 4-bit intermediate carry generated. Since product of a 4 x 4 multiplier is 8 bits long, in every step the least significant 4 bits correspond to the product and the remaining 4 bits are carried to the next

step. This process continues for 3 steps in this case. Similarly, 16 bit multiplier has four 8 x 8 multiplier and two 16 bit adders with 8 bit carry. Therefore we see that the multiplier is highly modular in nature. Hence it leads to regularity and scalability of the multiplier layout.

IV. ARCHITECTURE

Our design of Q-format signed multiplier includes Urdhava Tiryakbhyam integer multiplier [4] with certain modifications as follows. This multiplier is faster since all the partial products are computed concurrently. Considering a 16 bit Q15 multiplier, the product is also a Q15 number which is 16 bits long.

Firstly, if the MSB of input is 1 then it is a negative number. Therefore 2's complement of the number is taken before proceeding with multiplication. Since the MSB denotes sign it is excluded and a '0' is placed in this position while multiplying. A Q15 format multiplier consists of four 8 x 8 Urdhava multipliers and the resulting product is 32 bits long as shown in fig. 4. But the product of a Q15 number is also a Q15 number which should be 16 bits long. Therefore the 32 bit product is left shifted by 1 bit to remove the redundant sign bit and only the most significant 16 bits of this product are considered which constitute the final product. An xor operation is performed on the input sign bits to determine the sign of the result.

If the output is '1' it enables the conversion of the 16 bit final result to its 2's complement format indicating a negative product. Similarly, for a 32 bit Q31 format multiplier as shown in fig. 5, four 16 X 16 Urdhava multipliers are used and only the most significant 32 bits after left shifting by one bit are considered which constitute the final 32 bit Q31 format product. An xor operation similar to Q15 multiplier is used to change the result to 2's complement format if it is negative.

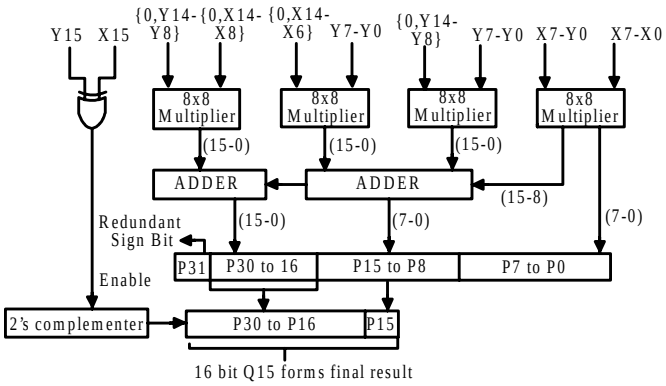

Figure. 4*.Architecture of a Q15 format m multiplier. multiplication of two Q15 numbers X and Y results in a Q15 product denoted by P in the figure.*

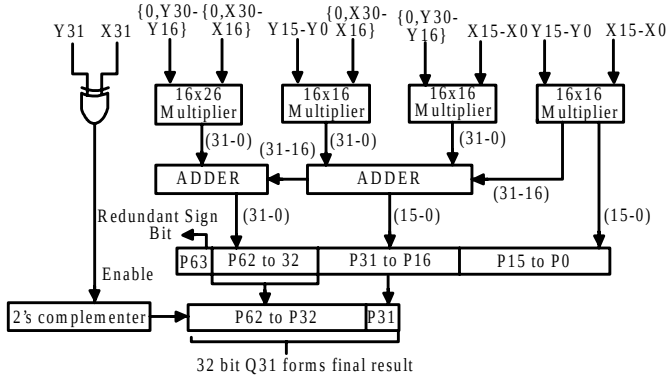

Figure .5 *Architecture of a Q31 format Multiplier.*

V. IMPLEMENTATION AND RESULTS

The proposed Urdhava Tiryakbhyam Q-format multiplier is designed using Verilog hard ware description language and structural form of coding. The basic block of both Q15 and Q31 multiplier is a 4 x 4 Urdhava Tiryakbhyam integer multiplier which in turn is made up of two 2 x 2 multiplier blocks. The design is completely synchronized by the clock. Further, the Q-format multipliers were also implemented using normal booth's algorithm. . The code is completely synthesized using Xilinx XST and implemented on device family Virtex-5, device XC5VL50, package FF324 with speed grade -2.

Simulation Results

The design was simulated using Isim on Xilinx ISE 12.2 version. For Q15 format multiplication as shown in figure. 6,

Input1 = -0.75 = 1010 0000 0000 0000

Input2 = - 0.25 = 1100 0000 0000 0000

Output = 0.1875 = 0001 1000 0000 0000.

For Q31 format multiplication as shown in figure. 7,

Input1= -0.666666 = 10101010101010101011000001000010

Input2 = 0.333333 = 00101010101010101010011111011111

Output = 11100011100011100011110010011110

Whose value is

-0.22222177777439355850219726556 25.

But the actual value of the product is -0.222221777778. Therefore precision loss is involved in this multiplication and is found to be 3.60644E-12 which is less than the resolution of Q31 representation i.e 2^{-31}. Thus it provides 32 bit accurate product which is acceptable for most of the DSP applications.

As shown in table 1, the comparison report

suggests that a Q31 format Urdhava Qformat multiplier is faster by 2.61 times than Normal Booth Multiplier . For a Q-15 format multiplier, as seen in table 2 the speed factor improvement is 1.84 times compared to booth multiplier.When Virtex-5 DSP48E slices were used with Normal Booth multiplier, Urdhava multiplier still proved to be faster indicating that it is the best choice for implementing faster multipliers on FPGA.

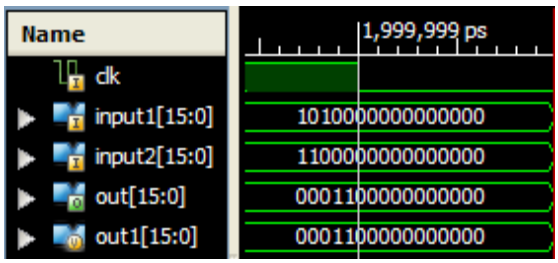

Figure : 6.*Q15multiplication*

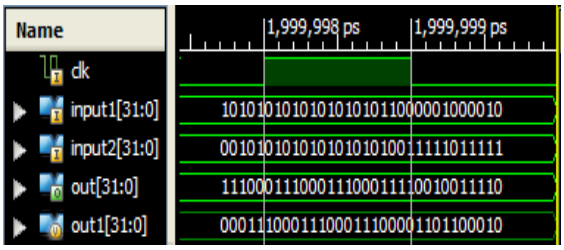

Figure : 7.*Q31multiplication*

Table-1

COMPARISON OF 32 BIT Q31-FORMAT MULTIPLIERS

	Maximum Frequency (in MHz)	**6-input Slice LUT Usage**	**Factor by which Urdhava Multiplier is faster**
Urdhava Multiplier	158.90	2710/19200	-------
Normal Booth Multiplier	60.88	3047/19200	2.61 times

Table-2

COMPARISON OF 16 BIT Q15-FORMAT MULTIPLIERS

	Maximum Frequency (in MHz)	**6-input Slice LUT Usage**	**Factor by which Urdhava Multiplier is Faster**
Urdhava Multiplier	236.18	662/19200	------
Normal Booth Multiplier	128.35	718/19200	1.84 times

Table -3

COMPARISON OF Q-FORMAT MULTIPLIERS USING VIRTEX 5 DSP48E BLOCKS

	Q15 format Maximum Frequency	Q31 format Maximum Frequency
NORMAL BOOTH MULTIPLIER using on board DSP48E blocks	128.35 MHz	60.88 MHz
Urdhava multiplier using LUT s only.	236.18 MHz	158.90 MHz
Speed factor Improvement	1.15 times	1.40 times

VI. CONCLUSION

This paper proposed a fast multiplier architecture for signed Q-format multiplications using Urdhava Tiryakbhyam method of Vedic mathematics. Since Q-format representation is widely used in Digital Signal Processors the proposed multiplier can substantially speed up the multiplication operation which is the basic hardware block. They occupy less area and are faster than the booth multipliers. Therefore the Urdhava Tiryakbhyam Q-format multiplier is best suited for signal processing applications requiring faster multiplications. Future work lies in the direction of introducing pipeline stages in the multiplier architecture for maximizing throughput.

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Clock Pair Shared Pulsed Flipflop

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ABSTRACT

Low power flip-flops which plays a vital role for the design of low-power digital systems. Flip flops and latches consume large amount of power due to redundant transitions and clocking system. In addition, the energy consumed by low skew clock distribution network is steadily increasing and becoming a larger fraction of the chip power. Almost, 30% -60% of total power dissipation in a system is due to flip flops and clock distribution network. In order to achieve a design that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops and latches. We survey a set of flip flops designed for low power and High performance.

Keywords

Flip Flop, Low Power, CMOS Circuit

INTRODUCTION

The major concerns of the VLSI designer were area, performance, cost and reliability. Power Consumption is determined by several factors including frequency f, supply voltage, data activity, capacitance, leakage and short circuit current. Circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short period

$$P_{short\,circuit} = 1_{short\,circuit} * Vdd$$

P leakage is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the sub threshold leakage current.

P leakage current = I leakage current * Vdd

EXISTING

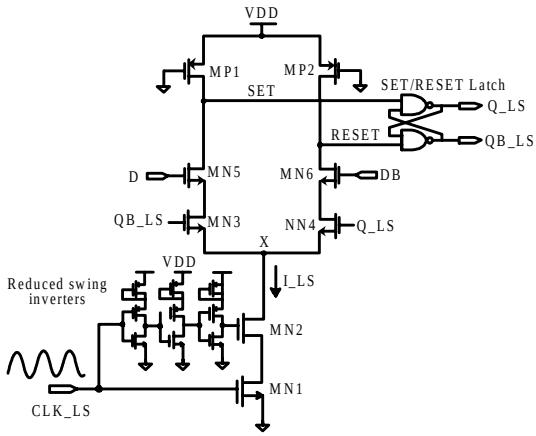


FIG1: *LS-DCCFF*

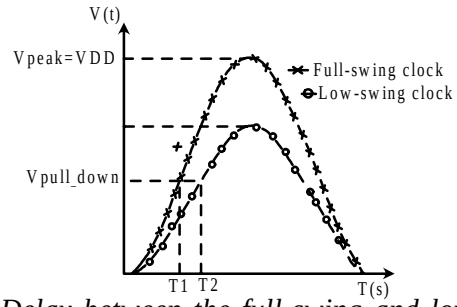


FIG2: Delay between the full-swing and low-swing Resonant clock signals to reach $V_{pull-down}$

$$T_{DQdelay} = T_2 - T_1$$

In existing system the clock signal is sinusoidal and the area is high in clock distribution network due to LC components and also the number of the clock transistors is high. To reduce the number of transistors and the area here used the clock signal is square signal. In this the delay, power consumption and area is determined with the help of simulation results and layout.

LOW POWER FLIP FLOP DESIGN

There are three source of power dissipation in digital complementary metal-oxide-semiconductor (CMOS) circuit. That is static power dissipation, dynamic power dissipation and short circuit power dissipation. Dynamic and short circuit power dissipation fall under the category of Transient Power Dissipation. Static power dissipation is due to leakage currents.

$$P = P_{dynamic} + P_{short\,circuit} + P_{leakage}$$ Dynamic Power is also called as switching Power. It is caused by continuous charging and discharging of output parasitic capacitance. Short circuit power is the result when pull up and pull down network will conduct simultaneously. Leakage power dissipation arises when current flow takes place from supply to ground in idle condition. Power consumption is directly proportional to supply voltage, frequency and capacitance.

DOUBLE EDGE TRIGGERING METHOD

Double clock edge triggering method reduces the power by decreasing frequency. Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be allow swing flip- flop. The low swing method reduces the power consumption by decreasing voltage.

In double edge triggering flip flop the number of clocked transistor is high than single edge triggering flip flop. This method is preferable to the circuits which consist of reduced number of clocked transistors. In dual edge triggering the flip flop is triggered in both edges of clock pulses. so the half of the clock operating frequency is enough and it will reduce the power consumption.

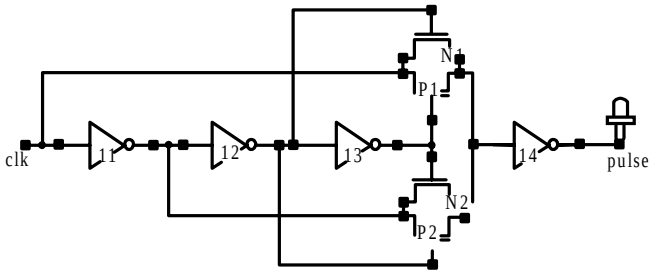


FIG3: *Dual Pulse Generator Circuit*

CLOCK PAIR SHARED PULSED FLIP FLOP

This low power flip flop is the improved version of Conditional Data Mapping Flip flop (CDMFF). It has totally19 transistors including 4 clocked transistors as shown in Figure 1. The N3 and N4 are called clocked pair which is shared by first and second stage. The floating problem is avoided by the transistor P1 (always ON) which is used to charge the internal node *X*. This flip flop will operate, when CLK and CLK db is at logic '1'. When D =1, Q = 0, Qb_kpr =1, N5 = OFF, N1= ON, the ground voltage will pass through N3, N4 and N1 then switch on the P2. That is Q output pulls up through P2. When D=0, Q=1, Qb_kpr=0, N5= ON, N1= OFF,Y=1, N2= ON, then Q output pulls down to zero through N2,N3 and N4.The flip flop output is depending upon the previous output Qand Qb_kpr in addition with clock and data input. So the initial condition should be like when D =1 the previous state of Q should be '0' and Qb_kpr should be '1'. Similarly whenD = 0 the previous state of Q should be '1' and Qb_kpr should be '0'. Whenever the D =1 the transistor N5 is idle, Whenever the D = 0 input transmission gate is idle.

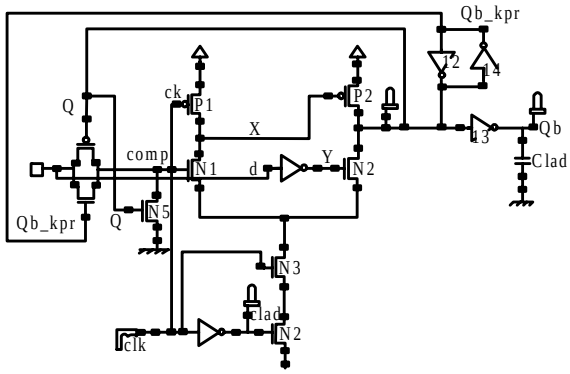


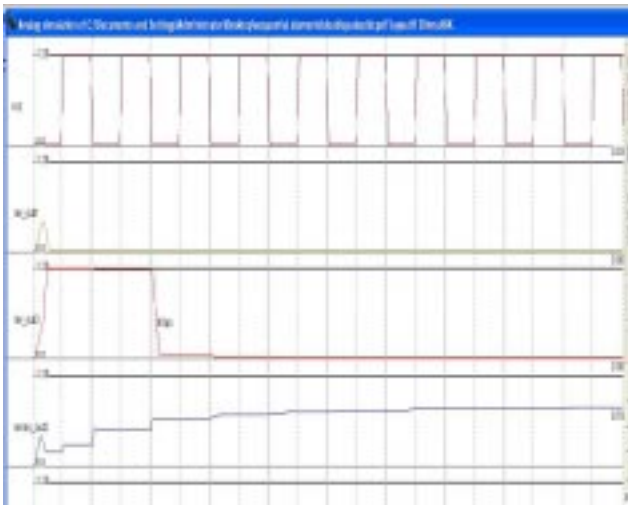
FIG4: *Clocked Pair Shared pulsed Flip Flop*

In high frequency operation the input transmission gate andN5 will acquire incorrect initial conditions due to the feedback from the output. The noise coupling occurred in the Q output due to continuous switching at high frequency. The glitch will be appearing in the Q output. It will propagate to the next stage which makes the system more vulnerable to noise. In order to avoid the above drawbacks and reduce the power consumption in proposed flip flop, we can make the flip flop output as independent of previous state. That is without initial conditions and removal of noise coupling transistors. In addition double edge triggering can be applied easily for power reduction to the proposed flip flop. It will be a less power consumption than other flip flops.

COMPARISON TABLE:

PARAMETERS	LS-DCCFF	CPSPFF
Power (w)	6.5	5.2
Delay(ps)	920	850
Area(m^2)	43	38

SIMULATION RESULTS



CONCLUSION

We conclude this paper by outlining an important set of guidelines which are the corner stone for low power flip-flop design methodology and low power flip-flop simulation. In general, low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for a long time. We have presented a survey and evaluation of low-power flip-flop circuits. Our experimental results enabled us to identify the power and performance trade-offs of existing flip-flop designs

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Implementation of STBC for MIMO Based on Alamouti Principle

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ABSTRACT

Abstract – Realization of multi input and multi output (MIMO) systems is highly essential for Wimax networks. Space–time block coding is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer.

In wireless communications the transmitted signal must traverse a potentially difficult environment with scattering, reflection, refraction and so on and may then be further corrupted by thermal noise. In the receiver STBC redundancy results in a higher chance of being able to use one or more of the received copies to correctly decode the received signal. The space–time coding combines all the copies of the received signal in an optimal way to extract as much information from each of them as possible.

In this project a computationally efficeint algorithm for space time block decoding will be implemented for FPGA based applications. The VHDL will be used for realization of the decoding alogrithm and other communication blocks.

The algorithm will be realized for Phase Shift Keying modulation (BPSK) scheme. The STBC encoder will also be realized in MATLAB/OCTAVE which generates the required appropriate codes for decoder. The work involves FPGA implementation of STBC decoder, and demodulator. Various sub blocks such as SIN/COS generators, multipliers, adders, encoding look up tables, complex arithmetic units etc will be implemented. These blocks will be realized in generic style to ensure scalability and reconfigurability of the STBC decoder design.

Modelsim xilinx edition (MXE) tool will be used for simulation and functional verification. Xilinx Synthesis technology (XST) will be used for FPGA synthesis. Timing analysis will be carried out to predict the maximum acheviable clock speeds for choosen Xilinx sparatan 3E FPGA device.

INTRODUCTION

Nowadays, there is a growing demand for providing high data rates and transmission quality in the condition of limited spectral resource and power consumption. With these requirements, several new technologies emerge, such as multiple-input multiple output (MIMO) technology, cooperative communication, ultra wideband (UWB) and cognitive radio.

Space-time coding as a primary MIMO technique which uses multiple antennas at both the transmitter and receiver sides are well known for its ability to resist the in?uence of wireless fading channel and provide higher capacity and better system performance than single link systems in wireless communications. Recently, it has been demonstrated that user-cooperation represents an effective way to introduce spatial diversity in wireless scenarios where we can not take the full bene?t of the uncorrelated channels from the multi-antenna systems. Cooperative diversity gains can be achieved through creating distributed virtual antennas across different terminals in the network. Taking advantage of the rich wireless propagation environment across multiple protocol layers in network architecture, we can obtain numerous opportunities to dramatically improve network performance. The theoretical analysis of such cooperative systems has attracted signi?cant interests and the study of practical architectures is a fertile area of research.

In Cooperative communication system each relay can play as a virtual antenna of the source. Laneman gave the basic algorithm and architecture of cooperative communication in his thesis. In this section, we present the computer simulation results about the STBC based cooperative communication systems. Virtual Alamouti STBC theory is employed in all these different cases. Slow Rayleigh fading channel and ideal channel estimation are assumed in the simulation. BPSK modulation and MRC/ MLD receiver are applied.

In this paper, we investigate the STBC based multi-antenna cooperative systems and provide the corresponding simulated performance under slow Rayleigh fading channel.

MULTI- INPUT MULTI OUTPUT (MIMO)

In radio, multiple-input and multiple-output, or MIMO is the use of multiple antennas at both the transmitter and receiver to improve communication performance. It is one of several forms of smart antenna technology. Note that the terms input and output refer to the radio channel carrying the signal, not to the devices having antennas.

MIMO technology has attracted attention in wireless communications, because it offers significant increases in data throughput and link range without additional bandwidth or transmit power. These business companies permit of facilitate their clients to use them for free. These business companies permit of facilitate their clients to use them for free. WiFi also rolled out for similar aims but WIMAX offer enhanced Quality of Service WiFi also rolled out for similar aims but WIMAX offer enhanced Quality of Service It achieves this by higher spectral efficiency (more bits per second per hertz of bandwidth) and link reliability or diversity (reduced fading).

Because of these properties, MIMO is an important part of modern wireless communication standards such as IEEE 802.11n (Wifi), 4G, 3GPP Long Term Evolution, WiMAX and HSPA+.

HISTORY OF MIMO

Wireless Standards

In the commercial arena, Iospan Wireless Inc. developed the first commercial system in 2001 that used MIMO with Orthogonal frequency-division multiple access technology (MIMO-OFDMA). Such private networks are expected to be the very last WIMAX application. Iospan technology supported both diversity coding and spatial multiplexing. In 2005, Airgo Networks had developed an IEEE 802.11n precursor implementation based on their patents on MIMO.

Following that in 2006,several companies (including at least Broadcom, Intel, and Marvell) have fielded a MIMO-OFDM solution based on a pre-standard for 802.11n WiFi standard. Also in 2006, several companies (Beceem Communications, Samsung, Runcom Technologies, etc.) have developed MIMO-OFDMA based solutions for IEEE 802.16eWiMAX broadband mobile standard. All upcoming 4G systems will also employ MIMO technology. Several research groups have demonstrated over 1 Gbit/s prototypes.

Functions of MIMO

MIMO can be sub-divided into three main categories

Precoding

It is multi-stream beamforming, in the narrowest definition. In more general terms, it is considered to be all spatial processing that occurs at the transmitter. In (single-layer) beamforming, the same signal is emitted from each of the transmit antennas with appropriate phase (and sometimes gain) weighting such that the signal power is maximized at the receiver input. The benefits of beamforming are to increase the received signal gain, by making signals emitted from different antennas add up constructively, and to reduce the multipath fading effect. In the absence of scattering, beamforming results in a well defined directional pattern, but in typical cellular conventional beams are not a good analogy.

When the receiver has multiple antennas, the transmit beamforming cannot simultaneously maximize the signal level at all of the receive antennas, and precoding with multiple streams is used. Because it offers significant increases in data throughput and link range without additional bandwidth or transmit power. These business companies permit of facilitate their clients to use them for free. Note that precoding requires knowledge of channel state information (CSI) at the transmitter.

Spatial multiplexing

It requires MIMO antenna configuration. In spatial multiplexing, a high rate signal is split into multiple lower rate streams and each stream is transmitted from a different transmit antenna in the same frequency channel. If these signals arrive at the receiver antenna array with sufficiently different spatial signatures, the receiver can separate these streams into (almost) parallel channels. Spatial multiplexing is a very powerful technique for increasing channel capacity at higher signal-to-noise ratios (SNR). The maximum number of spatial streams is limited by the lesser in the number of antennas at the transmitter or receiver. Spatial multiplexing can be used with or without transmit channel

knowledge. Spatial multiplexing can also be used for simultaneous transmission to multiple receivers, known as space-division multiple access. By scheduling receivers with different spatial signatures, good separability can be assured.

Diversity Coding

These techniques are used when there is no channel knowledge at the transmitter. In diversity methods, a single stream (unlike multiple streams in spatial multiplexing) is transmitted, but the signal is coded using techniques called space-time coding. The signal is emitted from each of the transmit antennas with full or near orthogonal coding.

Diversity coding exploits the independent fading in the multiple antenna links to enhance signal diversity. The maximum number of spatial streams is limited by the lesser in the number of antennas at the transmitter or receiver. Because there is no channel knowledge, there is no beamforming or array gain from diversity coding.

Spatial multiplexing can also be combined with precoding when the channel is known at the transmitter or combined with diversity coding when decoding reliability is in trade-off.

FORMS OF MIMO

Applications of MIMO

Spatial multiplexing techniques makes the receivers very complex, and therefore it is typically combined with Orthogonal frequency-division multiplexing (OFDM) or with Orthogonal Frequency Division Multiple Access (OFDMA) modulation, where the problems created by multi-path channel are handled efficiently. The IEEE 802.16e standard incorporates MIMO-OFDMA. The IEEE 802.11n standard, released in October 2009, recommends MIMO-OFDM.

MIMO is also planned to be used in Mobile radio telephone standards such as recent 3GPP and 3GPP2 standards. The maximum number of spatial streams is limited by the lesser in the number of antennas at the transmitter or receiver. In 3GPP, High-Speed Packet Access plus (HSPA+) and Long Term Evolution (LTE) standards take MIMO into account. Moreover, to fully support cellular environments MIMO research consortia including IST-MASCOT propose to develop advanced MIMO techniques, i.e., multi-user MIMO (MU-MIMO).

MIMO technology can be used in non-wireless communications systems. One example is the home networking standard ITU-T G.9963, which defines a powerline communications system that uses MIMO techniques to transmit multiple signals over multiple AC wires (phase, neutral and ground).

Space Time Block Coding (STBC)

It is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer. The fact that transmitted data must traverse a potentially difficult environment with scattering, reflection, refraction and so on and, as well as, be corrupted by thermal noise in the receiver means that some of the received copies of the data will be "better" than others. This redundancy results in a higher chance of being able to use one or more of the received copies of the data to correctly decode the received signal. In fact, STBC combines all the copies of the received signals in an optimal way to extract as much information from each of them as possible.

Maximum likelihood estimation

It was none other than R. A. Fisher who developed maximum likelihood estimation. Fisher based his work on that of Karl Pearson, who promoted several estimation methods, in particular the method of moments. While Fisher agreed with Pearson that the method of moments is better than least squares, Fisher had an idea for an even better method. It took many years for him to fully conceptualize his method, which ended up with the name maximum likelihood estimation.In 1912, when he was a third year undergraduate student, Fisher published a paper called "Absolute criterion for fitting frequency curves."

The concepts in this paper were based on the principle of inverse probability, which Fisher later discarded. Because Fisher was convinced that he had an idea for the superior method of estimation, criticism of his idea only fueled his pursuit of the precise definition. In the end, his debates with other statisticians resulted in the creation of many statistical terms we use today, including the word "estimation" itself and even "statistics". Finally, Fisher defined the difference between probability and likelihood and put his final touches on maximum likelihood estimation in 1922.

Mathematical Theory of Maximum Likelihood Estimation

Suppose we have flipped a coin three times and observed a sequence of events HHT. We know that flipping a coin is modeled by the binomial probability density function,

$$P(k;n,p)=\binom{n}{k}p^{k}(1-p)^{n-k}$$

where we have k successes out of n Bernoulli trials and we define the random variable K as either "heads"

or "not heads" on each toss. The parameter of this model is *p*, the probability of flipping a coin and getting heads. So we define

$$P(K=1)=p$$
$$P(K=0)=(1-p)$$

For our sequence HHT K1 = 1, K2 = 1, and K3 = 0, and since these trials are independent, we get

$$P(K_1=1\cap K_2=1\cap K_3=0)=P(K_1=1),P(K_2=1),P(K_3=0)$$

which means ,

$$P(K_1=1\cap K_2=1\cap K_3=0)=p^2(1-p)$$

Based on this data set, a good estimate for the mean of the binomial model is $\frac{2}{3}$

since $P(k)=\binom{n}{k}\frac{2^k}{3}\left(\frac{1}{3}\right)^{n-k}$

is much more likely to predict HHT than

$$P(k)=\binom{n}{k}\frac{1^k}{2}\left(\frac{1}{2}\right)^{n-k}$$

which is what we might have expected since most coins have a probability of getting heads of one half. But in this case, based on our known data, we expect to get heads two thirds of the time on future tosses with the same coin.

Properties of Estimators

The maximum likelihood estimator is just one of an infinite number of estimators. Perhaps, like Fisher we want to compare estimators to see if we can determine which one is best.

Since we have made sure to define an estimator as a random variable, then they each have their own expected value, and variance which allow us to make comparisons.

While with a point estimate you have no way of knowing how precise it is, with estimators you can specify a confidence interval. The larger the sample size, the greater the precision of the estimator. The experimental design can incorporate the necessary sample size to provide the desired amount of precision.

OVERVIEW OF ALAMOUTI SCHEME

The Alamouti scheme is the only orthogonal space-time block code using complex signals for two transmit antennas which provides full diversity of 2 and full rate of 1. For more 2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications than two transmit antennas, the goal is to design transmission codes that achieve full diversity at the highest possible rate with low decoding complexity. In our 2×2 MIMO implementation, we use two distinct training codes over 2 time multiplexed preamble slots at the transmitter. When one transmitter is sending training data in one time slot, the other is off. These 26-bit preambles are GSM training sequence codes (TSC) 0 and 1 [11]. The two transmitters then transmit 128 space-time encoded data symbols simultaneously before the cycle repeats. At the transmitter, the SASRATS transmitters are programmed to run a 2 transmit Alamouti encoding scheme, where two symbols, $s0, and s1$, are transmitted simultanously from two transmitters at time instant t. At time instant $t+T$, the symbols $-s_1^*$ and s_0^* are transmitted simultanously from the transmitters where * represents the complex conjugate. The transmission matrix is represented by

$$S=\begin{bmatrix} s_0 & s_1 \\ -s_1^* & s_0^* \end{bmatrix}$$

The transmitted symbols travel through 2 independent channels $h0$ and $h1$ to a receiver where noises $n0 and n1$ are added to the received signals. $h0 and h1$ are complex multiplicative distortions assumed constant across two consecutive symbols.

The complexity of the combiner and ML detector depends on type of modulation. Binary phase shift keyed (BPSK) symbols are the simplest to detect. Detection of non equal energy modulation schemes require channel estimates in the ML detector and has higher complexity. The present work considers BPSK and QPSK implementations only.

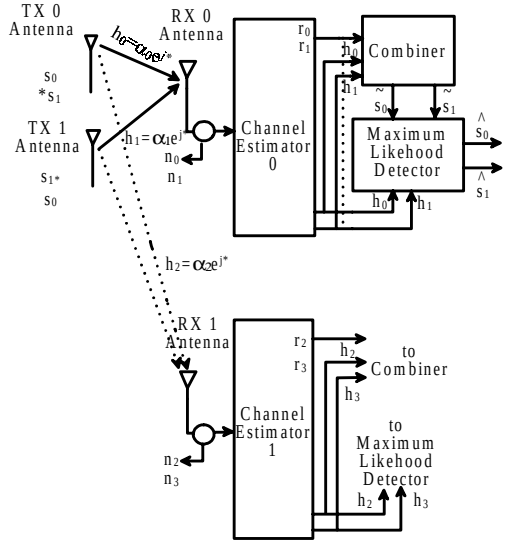

Figure: Block diagram of alamouti decoding implementation

Implementation of a MIMO 2 transmitter and 2 receiver Alamouti system, requires the estimation of 4 channel $(h_0, h_1, h_2 \text{ and } h_3)$, 2 at each receiver as shown in figure. In this situation, the output of combiner yields 2 outputs.

$$\tilde{s}_0 = h_0^* r_0 + h_1 r_1^* + h_2^* r_2 + h_3 r_3^*$$

where h_2 and h_3 are channel estimates from the second receiver. In the case of a 2×2 Alamouti implementation using PSK signals, the ML decoder remains unchanged except for the combiner. The combiner output s_0 is actually the sum of s_0 from receiver 0 and s_0 from receiver 1. Likewise, s_1 is actually the sum of s_1 from receiver 0 and s_1 from receiver 1. Thus a $2\times M$ Alamouti implementation can be easily implemented by summing together the appropriate combiner outputs from ?? receivers before feeding one ML detector. In an extended version of Alamouti for 4 transmitters , full rate is achieved but the system is half rank (quasi-orthogonal) with some loss in diversity as transmitted symbols cannot be fully decoupled. Tarokh's STBC scheme for 4 transmitters on the other hand, achieves complete orthogonality at half the full rate. Tarokhs scheme suffers no loss in diversity and receiver decoding is simpler as the transmitted symbols can be fully decoupled.

The complete design is implemented using a top down hierarchical schematic entry approach on the *Xilinx Integrated System Enviroment (ISE) Foundation* design tool.

VHDL code can also be integrated as a block with other schematic components if desired. We have also made extensive use*n* of various *Xilinx Core Generator* intellectual property(IP) modules incorporated within the ISE Foundation toolset to shorten design cycle time.

CONCLUSION

We have described the implementation of a real time maximum likelihood Alamouti decoder for use on our MIMO platform implemented on an FPGA using the Xilinx ISE tool and Core Generator IP modules. We have also experimentally verified the operation of the decoder in a closed Alamouti 2×1 diversity scheme using an RF channel simulator and also in an open 2×2 and 2×4 antenna based system under correlated channel conditions.

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High Speed Fault Injection Tool Implemented with Verilog HDL on FPGA for Testing Fault Tolerance Designs

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ABSTRACT

This paper presents an FPGA-based fault injection tool, called FITO that suppor several synthesizable fault models for dependability analysis of digital syster modeled by Verilog HDL. Using the FITO, experiments can be performed in real-time with good controllability and observability. As a case study, an Open RISC 1200 microprocessor was evaluated using an FPGA circuit. About 4000 permanent, transient, and SEUfaults were injected into this microprocessor. The results show that the FITO tool is more than 79 times faster than a pure simulation-based fault injection with only 2.5% FPGA area overhead.

KEY WORDS

Fault Tolerance Design , Gate level Fault Injection, Emulation Phase.

1. INTRODUCTION

Fault injection is mainly used to evaluate fault-tolerant mechanisms. In the last decade, fault injection has become a popular technique for experimentally determining dependability parameters of a system, such as fault latency, fault propagation and fault coverage [1]. Within the numerous fault injection approaches that have been proposed, there are two classifications for fault injection methods [2] hardware-based fault injection [3], [4], and software-based fault injection [5-11]. Software-based fault injection methods are divided into software-implemented fault injections (SWIFI) and simulation-based fault injections. In the simulation-based fault injection, faults are injected into the simulation model of the circuits using VHDL [1], [7], [8], [9] or Verilog[10], [11] languages. The main advantage of simulation-based fault injection as compared with other fault injection methods is the high observability and controllability[10],[2]. However, simulation-based fault injection methods are too time-consuming [2]. One way to provide good controllability and observability as well as high speed in the fault injection experiments is to use FPGA-based fault injection. An effective FPGA-based fault injection technique should support several properties as below

1. High controllability and observability,
2. High speed fault injection experiments with the target system running at full speed,
3. Capability of injecting permanent and transient faults,

All FPGA-based fault injection techniques that mentioned above inject faults at synthesizable VHDL models of the systems. Because of the use of Verilog hardware description language in implementation of many digital systems, the lack of FPGA-based fault injection tool which supports this hardware description language can be felt. This paper describes the FPGA-based fault injection tool, called, FITO which support all of the fourth properties as mentioned above and is based on Verilog description of the systems. FITO supports several fault models into RTL and Gate-level abstraction levels of the target system which has been described by the Verilog HDL[2]. For supporting high speed fault injection experiments, the fault injector part of FITO with low area overhead is implemented with synthesized microprocessor core inside the FPGA.

2. FAULT MODELS

Digital circuits which are developed by the hardware design languages have hierarchical modeling and can be implemented by several abstract levels. FITO performs fault injection experiments into the gate level and RTL[3] level of the circuits Verilog models.

The fault models which are introduced in gate level are the permanent and transient faults. In addition, bit-flip fault is proposed for the RTL level of the digital circuits.

Fault injection process can be done by applying some extra gates and wires to the original design description and modifying the target Verilog model of the system. One of these extra wires is the Fault Injection Signal (FIS) which playing the key role in the fault injection experiments. If a FIS takes the value 1, fault would be activated and if it takes the value 0, the fault would become inactive. For each FIS there would be a path through all levels of hierarchy to its modified circuit. After the modification, the final synthesizable Verilog description will be produced which is suitable to use in emulators. In the rest of the paper the synthesizable modification into the Verilog model of the circuit for supporting each fault model has been described.

2.1 GATE LEVEL FAULT INJECTION

FITO supports permanent and transient fault models by generating the modified Verilog source code of the target system for each fault model. The modified Verilog description of the circuit is synthesizable and can be used for FPGA-based fault injection experiments. For supporting the permanent faults in Verilog design, FITO nominates wires for fault injection and apply the FIS signal with one extra gate. So, by selecting the FIS signal high at fault injection time, the permanent fault into the specified wire will be injected.

Figure 1 shows the Verilog source code modification for supporting stuck-at fault models. FITO uses one timer for determining the fault injection time. It also uses another timer for finishing the fault injection experiment (workload execution). After reaching the fault injection time, the FIS signal will be high and another timer starts to count. As shown in figure 1 wire TX is the additional wire which is applied to the original design and the every wire namely X will be replaced by TX.

In addition, FITO can generate synthesizable modified Verilog source code of the target system for supporting transient faults. The modified circuit that is suitable for transient fault injection is shown in figure 2. After reaching the fault injection time, the FIS signal will be high and the timer which have been loaded with the duration of the transient fault injection start to count. Therefore, the FIS will be high (at logic 1) for the specified duration of time. As similar to the permanent fault, the additional wire (TX) will be used and each wire, namely X will be replaced with TX. Note, the fault injector part of FITO which is called Fault Injection Manager.

2.2 RTL LEVEL FAULT INJECTION

The fault model that is used by FITO at this level is bit-flip (or Single Event Upset). SEUs are the random events and may flip the content of the memory element at unpredictable times. FITO generate modified circuit for each memory element that is specified for fault injection. The modified circuit for supporting bit-flip fault model is shown in figure 3.

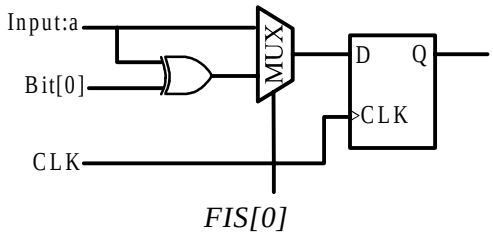

Figure 1 : *Synthesizable bit-Flip fault model*

For supporting the bit-flip fault model, FITO produces the additional signals such as Bit and FIS with one multiplexer. The Verilog synthesizable code for supporting this fault model is shown in figure 3. The inverted input will be goes to the flip-flop for the next clock that FIS and Bit are 1. FIS indicates the target register and the Bit will be high for the target register's bit. The fault injection manger part of FITO is responsible for setting and resetting the FIS and Bit signals.

3. THE FITO ENVIRONMENT

FITO is made of three main parts that every part is used in different fault injection phases. These parts are

1. Source Code Modifier & Fault List Generator
2. Fault Injection Manager
3. Result Analyzer

Source Code Modifier & Fault List Generator and Result Analyzer are the software parts of the FITO which are located on the host computer. On the other hand, Fault Injection Manager is responsible for performing the real-time fault injection. This hardware part is implemented on the FPGA board.

The fault injection process with FITO has been shown in Figure 4. As shown in this figure, each FITO's part that were mentioned before are used in different phases of the fault injection process. In the rest of the paper, each fault injection phases and the main work of each FITO's

part in these phases will be described in more details.

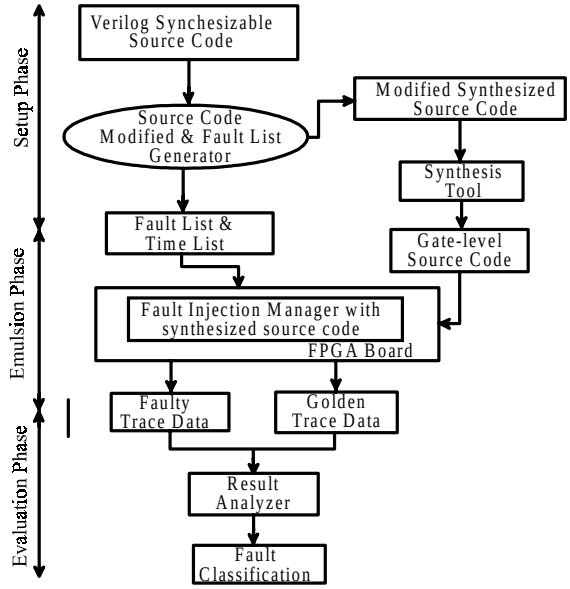

Figure 2 : *Fault injection process with FITO*

3.1 THE SETUP PHASE

The main objectives of this phase are achieving modified Verilog source codes of the original model that is synthesizable and generating correspond fault list for each fault injection experiments.

In setup phase the Verilog models have been given to the FITO. First, by selecting all or some of the considered fault models, the Source Code Modifier processes the Verilog model of the system. After user specifies the main module, a source navigator shows the wires and registers to user. After selecting the fault injection properties and the observation points, FITO generates the corresponding fault list, time list and the synthesizable modified source code. The synthesizable modified source code has additional flip-flops for each observation points.

Each time list indicates the time for triggering each fault injection experiment and the fault list is used for indicating the fault injection location. A typical fault list is described in figure 5. As shown in figure 5, the first bit of fault list is used for performing the fault injection experiment. In addition, two bits and eight bits are the inputs to decoder A and B. Outputs of decoder A and B are Bit[3:0] , FIS[255:0] which together indicate the bit position of the target register for bit-flip fault injection. The FIS[255:0] without Bit[3:0] are used for supporting permanent and transient fault models.

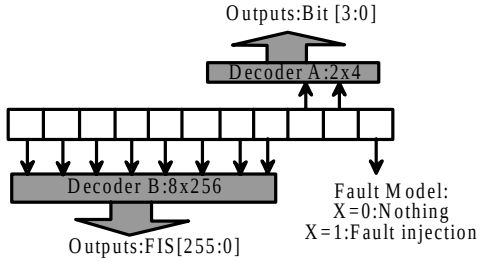

Figure 3 : *Fault list format*

Modified source code contains fault injection manager with modified circuit. So, the target system is suitable for fault injection experiments. Decoder A and B are the main parts of the fault injection manager.

After this step, the modified source code must synthesize with some synthesis tool and the gate level source code which is suitable for programming the FPGA will be produced. By using the gate level source code the FPGA will be programmed.

3.2 THE EMULATION PHASE

In the emulation phase, modified codes created by the previous phase are emulated. After emulating each experiment, the information of the observation points will be sent through the serial port. So, each experiment will have one trace file. Each trace file is created with the observation data points of each experiment. Results of this phase are providing 1) one fault free trace file (golden run trace file) and 2) faulty trace files which are generated by performing faulty experiments. During this phase, the Result analyzer part of FITO must be run from the user. This part sends each fault list and time list of the fault injection experiment to the fault injection manager. Then, the fault injection manager sends the contents of the observation points to the result analyzer. At the start of the fault injection experiments, the fault injection manager reset the first bit of fault list for creating the golden trace file. Then, each fault list and time list is sent to the FPGA board. After the fault injection the contents of the observation points are sent to the host computer for analyzing the system behavior.

3.3 THE EVALUATION PHASE

The main objective of this phase is the fault tolerance parameter estimation. It is done by result analyzer software part of FITO that is located on the host computer. Result analyzer estimates the dependability parameters by tracing differences between golden run and faulty trace files. Some facilities were developed for user interactions and for required fault tolerant parameter determination.

4. EXPERIMENTAL RESULTS

We developed the fault injection using the Altera DSP development board, equipped with Strati EP1S25F780C FPGA. An OpenRISC 1200 has been used as benchmark for FITO evaluation. The main reason for using OpenRISC 1200 is that it has synthesizable Verilog Description and intended for embedded systems, automotive, portable computer environments. In the experiments, two common workload programs are considered [10]. The matrix multiplication and the bubble sort. The workloads are coded in C and are compiled with GNU gcc compiler. So, after this step, the suitable code for the OpenRISC 1200 microprocessor will be generated. After this step we connected instruction and data memory to the processor with the workload which is loaded into the instruction memory.

Table 1: *Available and consumed FPGA resources (EP1S25F780C5)*

	#	%
Total Available LEs in the FPGA	25660	100
LEs used by the OpenRISC 1200	4769	18.58
LEs used by the OpenRISC 1200 + FI	5401	21.04

The faults are injected in different parts of the CPU modules of the OpenRISC 1200 core consisting of control unit, the genPC unit, the Instruction Fetch unit and the ALU unit. The total runtime of the matrix multiplication and bubble sort were 990 and 5890 clocks. In this experiment total 4000 permanent and transient faults injected at 100 random locations. For each location of the every fault, experiments were carried out 20 times with uniform distribution during the running of the each workload. The fault duration for transient faults were one clock period. The OpenRISC 1200 microprocessor emulated using 80 MHZ clock. The observation points are the address bus, data bus and the register file.

Table 2 shows the speed-ups. As shown in table 2, the resulted speed-up is workload dependent. This is because bubble sort workload generates more signal event than matrix multiplication.

Table 2: *The Resulted Speed-ups*

Workload	Simulation Time (sec)	Emulation Time (sec)	Speed-up
Matrix Multiplication	4605	51	90
Bubble Sort	13770	199	69

The fault propagation results, fault models for each module and the number of fault injection points have been shown in table 3.

As shown in table 3, different fault models are considered for each module of the OpenRISC 1200 microprocessor. The Ctrl unit (Control Unit) plays the key role in controlling the pipeline registers of the microprocessor. So, the transient fault model for the internal wires of this module was considered. The pc register which is the most important register of the system for controlling the flow of the workload is considered for bit-flip fault injection. So, the bit- flip fault model was considered for the Genpc unit that involves pc register.

5. C0MPARISON WITH FPGA-BASED FAULT INJECTION TOOLS

For estimating the main properties of FITO that were mentioned in section 1, a comparison between FITO and other fault injection tools is needed. FITO provides controllability over 255 wires and registers of the target microprocessor which is sufficient for having the control over the important wires and registers of the target microprocessor. Because of using the combinational logics (two decoders) and compacted fault and time lists the area overhead of FITO is very lower than the FIDYCO and FIFA and it uses one flip-flop for every fault injection location. The minimum 22% area overhead has been reported for FIFA tool.

CONCLUSION

This paper described the FPGA-based fault injection tool, called, FITO for evaluating the digital systems modeled by Verilog HDL. Fault injection with FITO is done by applying some extra gates and wires to the original design description and modifying the target Verilog model of the target system. FITO support some properties such as high speed, good controllability, good observability and low area overhead. As a case study, an OpenRISC 1200 have been evaluated on the EP1S25F780C FPGA and 4000 faults have been injected into this microprocessor. The effects of faults have been classified into control flow errors, data errors and failures activated. Results show that the FITO is more than 79 times faster than simulation-based fault injections with only 2.5% FPGA overhead.

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GDI Based Subthreshold Low Power D - Flipflop

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ABSTRACT

Energy performance requirements are forcing designers of next-generation syste to explore approaches to lease possible power consumption. Power consumption is majorly affected by power supply voltage. Scaling of power supply voltage is major factor to reduce power consumption. The technique to achieve ultra-low power is to operate the circuit with supply voltage less than threshold voltage. The region where supply voltage is less than threshold voltage is called sub threshold region. Ultra-low power consumption can be achieved by operating digital circuits at sub threshold region. Here proposed sub threshold circuit is based on GDI (Gate Diffusion Input) technique. GDI technique allows reducing power consumption, delay, area of the digital circuit while maintaining low complexity of logic design as compared to other CMOS (Complementary Metal Oxide Semiconductor) circuits.

KEY WORDS

Gate Diffusion Input technique, Sub threshold region, Ultra-low power .

INTRODUCTION

Increasing demand for battery-operated mobile platforms like laptops, cellular phones, etc., has led to the requirement for circuit designs to be more power aware. Scaling of power supply voltage is major factor to reduce the power consumption. Sub threshold operation has gained a lot of attention due to ultralow-power consumption applications requiring low to medium performance. It has also been shown that by optimizing the device structure, power consumption of digital sub threshold logic can be further minimized while improving its performance. To accomplish this task circuit with lower frequency should be operated in the weak inversion region or sub threshold region. Sub threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub threshold operation. The architectural technique described in this paper suggests a design to minimize area and capacitance by using Gate Diffusion Input (GDI) multiplexer.

As feature size of the CMOS (Complementary Metal Oxide Semiconductor) technology continues to scale down, leakage power has become an ever-increasing important part of the total power consumption of a chip. By utilizing the leakage current of devices working in sub threshold region, we propose a method to reduce the leakage power of D flip flops in this paper by using GDI technique. Implementing and simulating the D flip flop using the GDI technique and operating it in sub threshold or weak inversion region, reduces the area, and power consumption as well as power delay product w.r.t. the conventional CMOS circuits.

BASIC PRINCIPLE

SUB THRESHOLD REGION

Sub-threshold circuits operate with a supply voltage that is less than the threshold voltage of the transistor. Threshold voltage is the traditional level voltage and here the transistor operates essentially based on leakage. Traditional digital CMOS transistors run either in the ON state (saturation) or OFF state (sub threshold), the sub threshold circuits are either in an OFF state or an almost-ON state (still in sub threshold region but with weak inversion). The sub threshold region is particularly important for low voltage, low-power applications, such as when the MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) is used as switch in digital logic and memory applications,

because the sub threshold region describes how the switch turns on and off.

As power is related quadratic ally to the supply voltage, reducing the voltage to these ultra-low levels results in a dramatic reduction in both power and energy consumption in digital systems. Due to the exponential current-voltage (I-V) characteristics of the transistor, sub threshold logic gates provide near ideal voltage transfer characteristics. In the sub threshold region, the transistor input capacitance is less than that of strong inversion operation. The transistor input capacitance, in sub threshold, is a combination of intrinsic (oxide capacitance and depletion capacitance) and parasitic (overlap capacitance, fringing capacitances) of a transistor whereas the input capacitance in strong inversion operation is dominated by the oxide capacitance. Due to the smaller capacitance and lower supply voltage operation. Since the sub threshold leakage current is used as the operating current in sub threshold operation, these are not suitable for very high frequencies.

GATE DIFFUSION INPUT TECHNIQUE

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors This method is suitable for design of fast, low power circuits, reduced number of transistors while allowing simple top-down design. Gate-Diffusion-Input (GDI) design technique is an efficient alternative for the logic design in standard CMOS and SOI technologies .A basic GDI cell contains four terminals – G node (the common gate input of the NMOS(Negative channel Metal-Oxide Semiconductor) and PMOS(Positive channel Metal-Oxide Semiconductor) transistors), P node (the outer diffusion node of the PMOS transistor), N node (the outer diffusion node of the NMOS transistor), D node (the common diffusion of both transistors). P, N and D may be used as either input or output nodes, depending on the circuit structure shown in Fig.1.

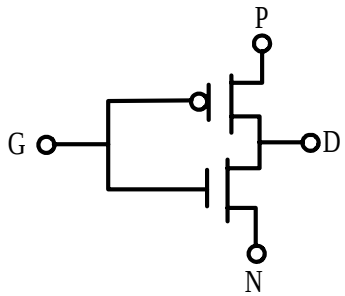

Figure1 : *Symbol of GDI cell*

Multiple-input gates can be implemented by combining several GDI cells .GDI enables simpler gates, lower transistor count, and lower power consumption in many implementations. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The overall area and complexity of the circuit is minimized using GDI technique. Most of the functions which are complex (6-12 transistors) in CMOS, are very simple (only 2 transistors per function) in GDI design method.

VARIOUS STAGES OF DESIGN

PREVIOUS DESIGN

The basic FF (Flip Flop) architecture reported in literature is a Master-Slave FF based on Gate-Diffusion Input (GDI) Multiplexers. GDI Multiplexers are composed of a single pair of transistors as shown in Figure.2 to the threshold voltage drop, but this phenomenon is substantially reduced in sub threshold operation. The design is composed of a pair of latches comprising a GDI multiplexer and a cross-coupled pair of inverters. The first multiplexer's (Mux1) selector is connected to the system clock (Clk) and its inputs are connected to the FF input (D) and the feedback loop. The inverted signal is the input to the second latch, with the feedback loop connected to the opposite input of the second multiplexer (Mux2). This topology creates a positive-edge triggered FF with a reduced Propagation delay due to the single inversion required before the output (Q) is ready. In addition, cell sizing can be used to optimize the timing properties of the cell, but shouldn't affect the operation of the circuit due to incorrect rationing or process variations.

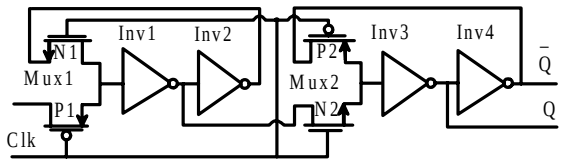

Figure2 : *Basic Flip Flop Diagram with GDI Multiplexer*

IMPROVED DESIGN

The improved design shown in Fig.3 that can reduce the area even further and improve the setup time. This is achieved by removing the first stage feedback inverter and passing the feedback from the second stage instead. The improved design, shown in Fig.3, comprises 10 transistors, In order to function correctly; this FF requires a delay on the clock fed to the selector of *Mux1*. Without this delay, the selected input of the Mux1 would toggle on the positive-edge of the clock before the updated value had arrived at its feedback input. Resistor can be used here as a delay element. The resistor area, on the other hand, depends very strongly on the technology which is used to fabricate the resistor on the chip. For fabricating of resistor using

standard PMOS resistor using the standard MOS process such as Diffused resistor and poly silicon resistor. The diffused resistor is fabricated, as name implies, as an isolated n type or P type diffusion region with one contact on each end. The resistance is determining by the doping density of the diffusion region and the dimension. The placement of this resistor structure on chip, commonly in a serpentine shape for compactness, requires significantly large area than the driver MOSFET. An alternative approach to save silicon area is to fabricate the load resistor using un doped poly silicon. In conventional poly gate MOS technology, the poly silicon structures forming the gates of transistor and the interconnect lines are heavily doped in order to reduce resistivity. But one drawback of this approach is that the resistance value cannot be controlled very accurately.

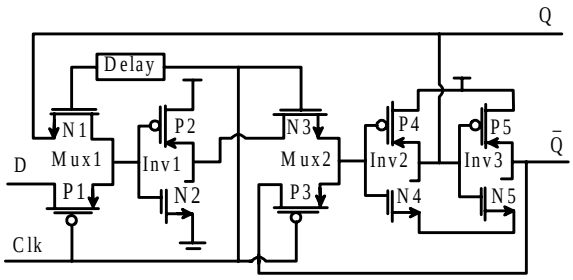

Figure3 : *Basic Schematic of Improved Flip Flop*

MODIFIED FLIPFLOP DESIGN

The basic flip flop design is further modified to achieve lesser power consumption. The modified circuit is shown in Fig.4. Here PMOS is used as a delay element. This FF comprises 11 transistors, a relatively small number, substantially reducing area and capacitance. In addition, the clock load of this design is only 4 transistor gates. The cross coupled inverters ensure that strong signals are passed from the multiplexers and block any reverse currents through the multiplexers. The PMOS transistor used in the modified circuit has high on resistance.

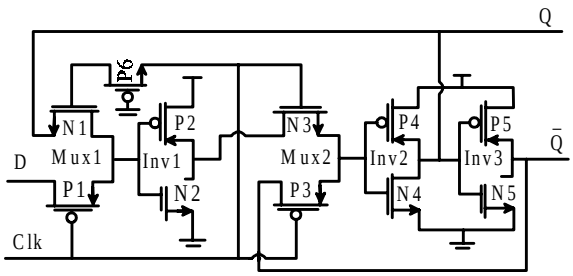

Figure4 : *Modified D Flip-Flop circuit using PMOS as delay element*

PROPOSED D FLIPFLOP DESIGN

The NMOS of the proposed circuit shown in Fig.5 is delay element. Without this delay, the selected input of theMux1 would toggle on the positive-edge of the clock before the updated value had arrived at its feedback input. NMOS is preferred over PMOS as NMOS has less on resistance and hence shows less power consumption. From the simulation results reveals that proposed circuit shows least power consumption as compared to all other circuits. This D flip flop require a delay on the clock fed to the selector of Mux1. In this case, the Inv1 could switch and change the state of the entire FF. Mux1 should toggle only after the Q (the feedback input of Mux1) reaches the sufficient level. Here NMOS provides sufficient delay so that until feedback has reached at the input of theMUX1.The presence of NMOS transistor would ensure that the MUX1 should toggle only when the output is generated at the positive edge of the clock. After this input is provided to MUX2 and the slave latch is enabled. This added delay is necessary for right operation of the flip flop.

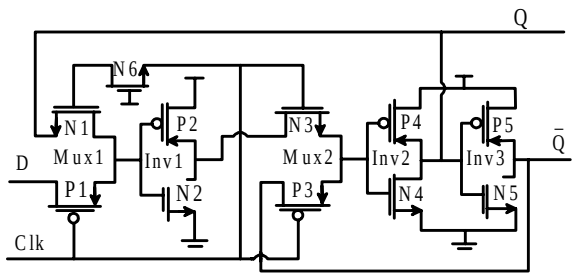

Figure5 : *Proposed D Flip-Flop circuit using NMOS as delay element*

SIMULATION RESULTS

SIMULATION ENVIRONMENT

The characterization of the flip-flop has been achieved by simulation on a 90 nm standard CMOS process. To establish an impartial testing environment each circuit have been tested on the same input patterns. The simulation is carried out by TSPICE using the BSIM4 predictive models at tanner EDA tool. All flip-flops are simulated in weak inversion region i.e. sub threshold with a threshold voltage of $V_{tn} = 0.17V$ and $V_{tp} = -0.19V$ and power supply voltage ranging from 110mVdown to 170mV.

SIMULATION COMPARISON

The proposed design circuit and previous design are simulated and compared for different V_{dd} (where the V_{dd} used in operation is below the threshold voltage of the PMOS and NMOS transistors) and operating frequency in terms of power consumption. Figure. 5 and Figure. 6shows the power at various values of V_{dd} and Frequency.

For all the values of V_{dd} and frequency, the GDI MUX based Flip-Flop yield less power consumption than GDI cell based Flip-Flop.

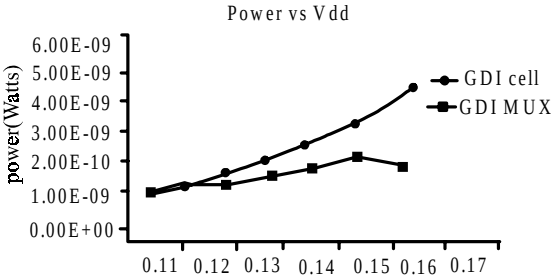

Figure5 : *Power vs Vdd of GDI cell and GDI MUX based Flip-Flop at weak inversion region*

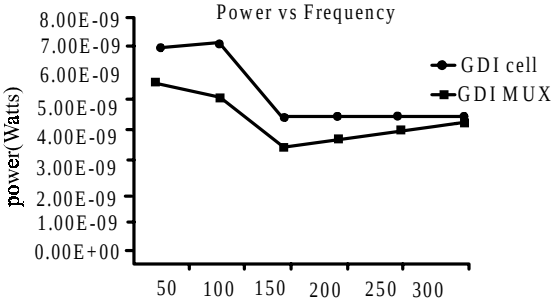

Figure 6 : *Power vs Frequency of GDI cell and GDI MUX based Flip-Flop at weak inversion region.*

Figure.7 and Fig.8 shows the comparison between GDI MUX based Flip-Flop with proposed D Flip-Flop Circuit. The proposed circuit shows less power consumption at different values of V_{dd} and Frequency.

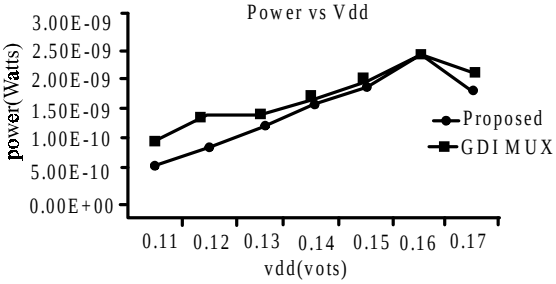

Figure 7 : *Power vs* V_{dd} *of GDI MUX based Flip-Flop and Proposed D flip flop circuit at Weak inversion region.*

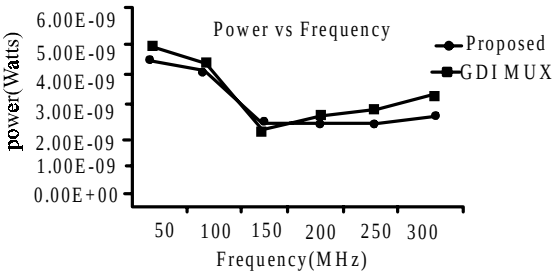

Figure 8. Power vs Frequency of Proposed D Flip-Flop and GDI MUX based Flip-Flop at Weak inversion region.Figure.9 and Figure.10 shows the power comparison of modified and proposed circuit at different values of frequency and V_{dd}*. Proposed circuit has less power consumption than modified circuit.*

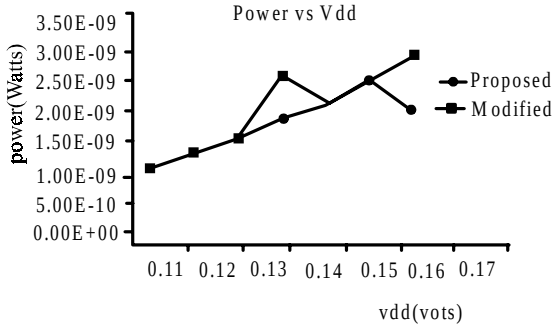

Figure 9 : *Power vs* V_{dd} *of Proposed D Flip-Flop and Modified D Flip-Flop circuit at Weak inversion region.*

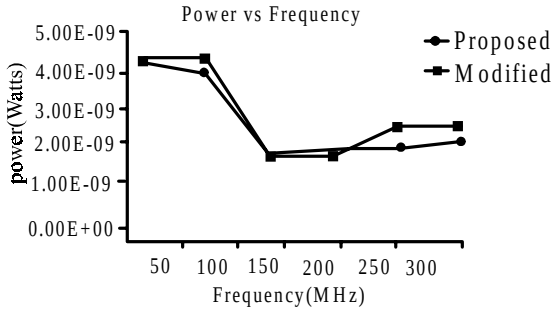

Figure10 : *Power vs Frequency of Proposed D Flip-Flop and Modified D Flip-Flop circuit at Weak inversion region.*

CONCLUSION

Digital logic sub threshold operation is introduced briefly as a means to achieve very high energy savings, and ultra-low power for systems which do not have high performance requirements. However, due to the high sensitivity of the sub threshold circuits to process variations, it is imperative to use innovative design techniques to improve circuit robustness. Sub threshold operation is suited for circuits which have low frequency requirements. Sub threshold region compared to the super threshold region such as exponential dependence of current on gate voltage, lower intrinsic gate capacitance. Because of these differences, conventional design techniques may yield suboptimal results. Comparisons show that proposed circuit is the best. The experimental results verify that GDI is superior to other styles.

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FPGA Implementation of High Speed AES Algorithm for Improving The System Computing Speed

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ABSTRACT

An implementation of high speed AES algorithm based on FPGA is presented in this paper in order to improve the safety of data in transmission. The mathematical principle, encryption process and logic structure of AES algorithm are introduced .so as to reach the purpose of improving the system computing speed, the pipelining and parallel processing methods were used. However Field programmable Gate Arrays (FPGAs) offer a quicker, more customizable solution. This research investigates the AES algorithm with regard to FPGA and the Very High Speed Integrated Circuit Hardware Description Language (VHDL). Software is used for simulation and optimization of the synthesizable VHDL code. All the transformations of both Encryption and Decryption are simulated using an iterative design approach in order to minimize the hardware consumption.

Keywords

AES algorithm (encryption, decryption), key expansion, hardware implementation.

1. INTRODUCTION

The National Institute of Standards and Technology (NIST), solicited proposals for the Advanced Encryption Standard, (AES). The AES is a Federal Information Processing Standard, (FIPS), which is a cryptographic Algorithm that is used to protect electronic data. The AES algorithm is a symmetric block cipher that can Encrypt, (encipher), and decrypt, (decipher), information. Encryption converts data to an unintelligible form called cipher-text. Decryption of the cipher-text converts the data back into its original form, which is called plaintext. The AES algorithm is capable of using cryptographic keys of 128, 192, and 256 bits to encrypt and decrypt data in blocks of bits.

Cryptography plays an important role in the security of data. It enables us to store sensitive information or transmit it across insecure networks so that unauthorized persons cannot read it. The urgency for secure ex-change of digital data resulted in large quantities of different encryption algorithms which can be classified into two groups: asymmetric encryption algorithms (with public key algorithms) and symmetric encryption algorithms (with private key algorithms). Symmetric key algorithms are in general much faster to execute electronically than asymmetric key algorithm.

The algorithm is composed of three main parts: Cipher, Inverse Cipher and Key Expansion. Cipher converts data to an unintelligible form called cipher text while Inverse Cipher converts data back into its original form called plaintext. Key Expansion generates a Key Schedule that is used in Cipher and Inverse Cipher procedure. Cipher and Inverse Cipher are composed of specific number of rounds (Table 1).

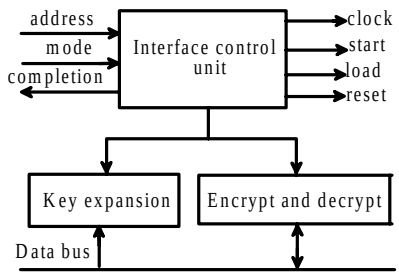

Figure 1: *AES module Architecture*

For the AES algorithm, the number of rounds to be performed during the execution of the algorithm is dependent on the key length.

Table.1

	Key Length (Nk words)	Block Size (Nb words)	Number of Rounds (Nr)
AES-128	4	4	10
AES-192	6	4	12
AES-256	8	4	14

Key-Block-Round combinations

AES operates on a 4x4 array of bytes (referred to a s "state"). The algorithm consists of performing four different simple operations.

These operations are

- **Sub Bytes**
- **Shift Rows**
- **Mix Columns**
- **Add Round Key**

Sub Bytes perform byte substitution which is derived from a Multiplicative inverse of a finite field.

Shift Rows shifts elements from a given row by an offset Equal to the row number.

Mix Columns step transforms each column using an Invertible linear transformation.

Add Round: Key step takes a 4x4 block from a expanded key

(Derived from the key), and XORs it with the "state".

AES is composed of four high-level steps. These are:

1. Key Expansion
2. Initial Round
3. Rounds
4. Final Round

The Key Expansion step is performed using key schedule. The Initial Round consists only of an Add Round Key operation. The Rounds step consists of a Sub Bytes, Shift Rows, Mix Columns, and an Add Round Key operation. The number of rounds in the Rounds step varies from 10 to 14 depending on the key size. Finally, the Final Round performs a Sub Bytes, Shift Rows, and an add Round key operations

Decryption in AES is done by performing the inverse operations of the simple operations in reverse order. However, as shown later on in this paper, because of the block cipher mode of operation used, decryption is Implemented but never used.

II. THE AES ALGORITHM

The AES encryption and decryption processes for a 128-bit plain text block are shown in Figure. 2 and 3. The AES Algorithm specifies three encryption modes: 128-bit, 192-bit, and 256-bit. Each cipher mode has a corresponding number of rounds Nr based on key length of Nk words .The state block size, termed Nb, is constant for all encryption modes. This 128-bit block is termed the state. Each state is comprised of 4 words. A word is subsequently defined as 4 bytes. Table1 Shows the possible key/state block/round combinations.

A. Encryption Process

The Encryption and decryption process consists of a number of different transformations applied consecutively over the data block bits, in a fixed number of iterations, called rounds. The number of rounds depends on the length of the key used for the encryption process. For key length of 128 bits, the number of iteration required are10. (Nr = 10). As shown in Figure. 2, each of the first Nr-1 rounds consists of 4 transformations: Sub Bytes (), Shift Rows (), Mix Columns () & Add Round Key ().

Fig: Structure of AES Encryption and Decryption process

The four different transformations are described in detail below

1) Sub Bytes Transformation (SB)

It is a non-linear substitution of bytes that operates independently on each byte of the State using a substitution table (S box). This S-box which is Invertible is constructed by first taking the multiplicative Inverse in the finite field GF (28) with irreducible Polynomial m(x) = x8 + x4+ x3 + x + 1. The element {00} is mapped to it. Then affine transformation is applied (over GF (2)).

2) Shift Rows Transformation (SR)

Cyclically shifts the rows of the State over different offsets. The operation is almost the same in the decryption process except for the fact that the shifting offsets have different values.

3) Mix Columns Transformation (MC)

This transformation operates on the State column-by-column, treating each column as a four-term polynomial.

The columns are Considered as polynomials over GF (28) and multiplied by modulo x4 + 1 with a fixed polynomial a(x) = {03} x3+ {01} x2+ {01} x+ {02}.

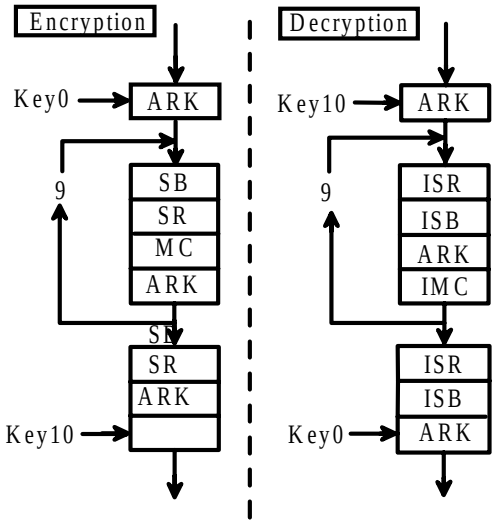

Figure : *Block diagram representation of AES algorithm (Decryption and Encryption)*

4) Add Round Key Transformation (ARK)

In this transformation, a Round Key is added to the State by a simple bitwise XOR operation. Each Round Key consists of Nb words from the key expansion.

Those Nb words are each added into the columns of the State. Key Addition is the same for the decryption process. Figure. AES Encryption and Decryption Process

Key Expansion: Each round key is a 4-word (128-bit) array generated as a product of the previous round key, a constant that changes each round, and a series of S-Box lookups for each 32-bit word of the key The key schedule Expansion generates a total of Nb (Nr+1) words.

B. Decryption Process

For decryption, the same process occurs simply in reverse order – taking the 128-bit block of cipher text and converting it to plaintext by the application of the inverse of the four operations. Add Round Key is the same for both encryption and decryption. However the three other functions have inverses used in the decryption process: Inverse Sub Bytes, Inverse Shift Rows, and Inverse Mix Columns.

This process is direct inverse of the Encryption process. All the transformations applied in Encryption process are inversely applied to this process. Hence the last round values of both the data and key are first round inputs for the Decryption process and follows in decreasing order.

III. IMPLEMENTATION

The AES algorithm is implemented using VHDL coding in Xilinx ISE 9.2. First, the algorithm is tested by encrypting and decrypting a single 128 bit block. After having an operational block cipher, the next step is to embed this block cipher in a block cipher modes of operation.

Cipher feedback (CFB) shown in Figure 4 and Figure 5, is chosen since the message does not have to be padded to a multiple of the cipher block size while preventing some manipulation of the cipher text.

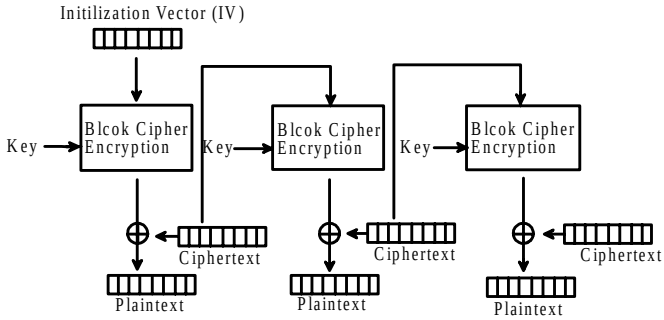

Figure 4: *Encryption using Cipher Feedback (CFB*

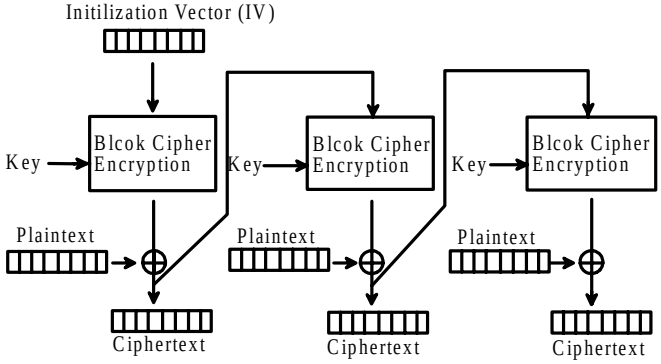

Figure 5: *Decryption using Cipher Feedback (CFB)*

IV. SIMULATION RESULT

A. Encryption Process (Cipher)

AES block length/Plain Text = 128bits (Nb = 4)

Key length = 128 bits (Nk = 4);

No. of Rounds = 10(Nr = 10)

Plain Text :00112233445566778899aabbccddeeff

Key : 000102030405060708090a0b0c0d0e0f

Output/Cipher Text: 69c4e0d86a7b0430d8cdb78070b4c55a

Figure 6 represents the waveforms generated by the 128- bit complete encryption Process. The inputs are clock1 & clock2, Active High reset, 4-bit round, and 128-bit state & key as a standard logic vectors, whose output is the 128-bit cipher (encrypted) data.

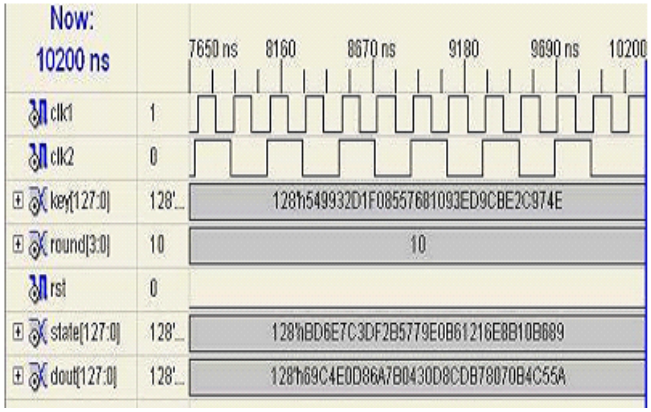

Figure 6: *Simulation Waveforms of final round of Encryption process*

B. Decryption Process (Inverse Cipher)

AES block length/Cipher Text = 128bits (Nb = 4)

Key length = 128 bits (Nk = 4);

No of Rounds = 10(Nr = 10)

Input/CipherText: 69c4e0d86a7b0430d8cdb78070b4c55a

Key : 000102030405060708090a0b0c0d0e0f

Output/Plain Text : 00112233445566778899aabbccddeeff

Figure 7 represents the waveforms generated by the 128- bit complete decryption Process. The inputs are clock1 & clock2, Active High reset, 4-bit round, and 128-bit state & key as standard logic vectors, whose output is the 128-bit plain text (decrypted data).

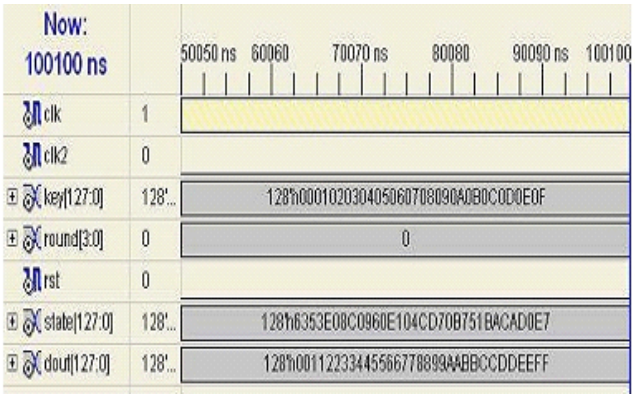

Figure 7: *Simulation Waveforms of final round of Decryption process*

V. TESTING AND VERIFICATION

The synthesis & mapping results of AES design are summarized in Table 2

Target FPGA device	Vertex XCV600BG 560-6
Optimization goal	Speed
Maximum Operating Freq	140.390 MHz
No. Of slices	1853 out of 6912(26%)
No. Of Slice flip flops	512 out of 13824(3%)
No. Of 4-i/p LUTs	3645 out of 13824(26%)
No. Of bonded IOBs	391 out of 408 (95%)
No. Of GCLK	2 out of 4(50%)
256x8-bit ROM	20
Encryption/Decryption Throughput	352 Mbps
Total memory uses	130248 Kbytes

Table 2: *Results of FPGA Implementation of AES*

The parameter that compares AES candidates from the Point of view of their hardware efficiency is Throughput. Encryption / Decryption Throughput = block size frequency total clock cycles. Thus, Throughput = 128 x 140.390MHz/51 = 352 Mbits/sec.

VI. CONCLUSION

The Advanced Encryption Standard algorithm is an iterative private key symmetric block cipher that can process data blocks of 128 bits through the use of cipher keys with lengths of 128, 192, and 256 bits. An efficient FPGA implementation of 128 bit block and 128 bit key AES cryptosystem has been presented in this Paper. Optimized and Synthesizable VHDL code is developed for the implementation of both 128 bit data Encryption and decryption process & description is verified using ISE 8.1 functional simulator from Xilinx. All the transformations of algorithm are simulated using an iterative design approach in order to minimize the hardware consumption. Each program is tested with some of the sample vectors provided by NIST. The throughput reaches the value of 352Mbit/sec for both encryption and decryption process with Device XCV600 of Xilinx Vertex Family.

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Weighted Pattern Generator for Fault Detection

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ABSTRACT

The hardware overhead and fault coverage of a circuit is an important problem in integrated circuits and Systems. To overcome this problem Accumulators based test pattern generator is utilized to test integrated circuits and systems .For integrated circuits, the weights are defined based on subsequences of test patterns. Here we reduce the number of test vectors to overcome the faults so that the fault coverage is maximum. In order to reduce the power and testing time we can use three weights namely 0, 1, and 0.5. This scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, Comparisons with previously presented schemes indicate that the proposed scheme compares favorably with respect to the required hardware.

Keywords

Memory BIST, Address Generation, ALU-based implementation.

I. INTRODUCTION

Pseudorandom built-in self test (BIST) generators have been widely utilized to test integrated circuits and systems. The arsenal of pseudorandom generators includes, among others, linear feedback shift registers (LFSRs) [1], cellular automata [2], and accumulators driven by a constant value [3]. For circuits with hard-to-detect faults, a large number of random patterns have to be generated before high fault coverage is achieved. Therefore, weighted pseudorandom techniques have been proposed where inputs are biased by changing the probability of a "0" or a "1" on a given input from 0.5 (for pure pseudorandom tests) to some other value [10], [12].

Weighted random pattern generation methods relying on a single weight assignment usually fail to achieve complete fault coverage using a reasonable number of test patterns since, although the weights are computed to be suitable for most faults, some faults may require long test sequences to be detected with these weight the assignments if they do not match their activation and propagation requirements. Multiple weight assignments have been suggested for the case that different faults require different biases of the input combinations applied to the circuit, to ensure that a relatively small number of patterns can detect all faults[4]. Approaches to derive weight assignments for given deterministic tests are attractive since they have the potential to allow complete coverage with a significantly smaller number of test patterns [10]. In order to reduce, minimize the hardware implementation cost, other schemes based on multiple weight assignments utilized weights 0, 1, and 0.5. This approach boils down to keeping some outputs of the generator steady (to either 0 or 1) and letting the remaining outputs change values (pseudo-) randomly (weight 0.5). This approach, apart from reducing the hardware overhead has beneficial effect on the consumed power, since some of the circuit under test (CUT) inputs (those having weight 0 or 1) remain steady during the specific test session [30]. Pomeranz and Reddy [5] proposed a 3-weight pattern generation scheme relying on weights 0, 1, and 0.5. The choice of weights 0, 1, and 0.5 was done in order to minimize the hardware implementation cost. Wang [2], [8] proposed a 3-weight random pattern generator based on scan chains utilizing weights 0, 1, and 0.5, in a way similar to [5]. Recently, Zhang *et al.* [9] renovated the interest in the 3-weight pattern generation schemes, proposing an efficient compaction scheme for the 3-weight patterns 0, 1, and 0.5. From the above we can conclude that 3-weight pattern generation based on weights 0, 1, and 0.5 has practical interest since it combines low

Current VLSI circuits, e.g., data path architectures, or digital signal processing chips commonly contain arithmetic modules [accumulators or arithmetic logic units

(ALUs)]. This has fired the idea of arithmetic BIST (ABIST) [6]. The basic idea of ABIST is to utilize accumulators for built-in testing (compression of the CUT responses, or generation of test patterns) and has been shown to result in low hardware overhead and low impact on the circuit normal operating speed [2]–[5]. In [6], Manich *et al.* presented an accumulator-based test pattern generation scheme that compares favorably to previously proposed schemes. In [7], it was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have acceptable pseudorandom characteristics, if the input pattern is properly selected. However, modules containing hard-to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns [4], [12].

In order to overcome this problem, an accumulator-based weighted pattern generation scheme was proposed in [11]. The scheme generates test patterns having one of three weights, namely 0, 1, and 0.5 therefore it can be utilized to drastically reduce the test application time in accumulator-based test pattern generation. However, the scheme proposed in [11] possesses three major drawbacks: 1) it can be utilized only in the case that the adder of the accumulator is a ripple carry adder; 2) it requires redesigning the accumulator; this modification, apart from being costly, requires redesign of the core of the data path, a practice that is generally discouraged in current BIST schemes; and 3) it increases delay, since it affects the normal operating speed of the adder.

In this paper, a novel scheme for accumulator-based 3-weight generation is presented. The proposed scheme copes with the inherent drawbacks of the scheme proposed in [11]. More precisely: 1) it does not impose any requirements about the design of the adder (i.e., it can be implemented using any adder design); 2) it does not require any modification of the adder; and hence, 3) does not affect the operating speed of the adder. Furthermore, the proposed scheme compares favorably to the scheme proposed in [11] and [12] in terms of the required hardware overhead. This paper is organized as follows. In Section II, the idea underlying the accumulator-based 3-weight generation is presented. In Section III, the design methodology to generate the 3-weight patterns utilizing an accumulator is presented. In Section IV, the proposed scheme is compared previously proposed ones. Finally, Section V, concludes this paper.

Test vector	Inputs A[4:0]
T1	00101
T2	01010
T3	10010
T4	11111

TABLE I

TEST SET FOR THE C17 BENCHMARK

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	0	0	1	1	0	$C_{out} = C_{in}$
3	0	1	0	1	0	$C_{out} = C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	1	0	1	0	1	$C_{out} = C_{in}$
7	1	1	0	0	1	$C_{out} = C_{in}$
8	1	1	1	1	1	

TABLE II

TRUTH TABLE OF THE FULL ADDER

II. ACCUMULATOR-BASED 3-WEIGHT PATTERN GENERATION

We shall illustrate the idea of an accumulator-based 3-weight pattern generation by means of an example. Let us consider the test set for the c17 ISCAS benchmark [12], [3] given in Table I. Starting from this deterministic test set, in order to apply the 3-weight pattern generation scheme, one of the schemes proposed in [5], [8], and [9] can be utilized. According to these schemes, a typical weight assignment procedure would involve separating the test set into two subsets, S1 and S2 as follows: S1 = {T1 , T4} , S2 = {T2 , T3} The weight assignments for these subsets is W(S1) = {-,-,1,-,1} and W(S1) = {-,-,0,1,0} where a "-" denotes a weight assignment of 0.5, a "1" indicates that the input is constantly driven by the logic "1" value, and "0"indicates that the input is driven by the logic "0" value. In the first assignment, inputs A[2], and A[0] are constantly driven by "1", while inputs A[4], A[3], A[1] are pseudo randomly generated (i.e., have weights 0.5). Similarly, in the second weight assignment (subset S2), inputs A[2] and A[0] are constantly driven by "0", input A[1] is driven by "1" and inputs A[4] and A[3] are pseudo randomly generated. The above reasoning calls for a configuration of the accumulator, where the following conditions are met: 1) an accumulator output can be constantly driven by "1" or "0" and 2) an accumulator cell with its output constantly driven to "1" or "0" allows the carry input of the stage to transfer to its carry output unchanged. This latter condition is required in order to effectively generate pseudorandom patterns in the accumulator outputs whose weight assignment is "-".

III. DESIGN METHODOLOGY

The implementation of the weighted-pattern generation scheme is based on the full adder truth table, presented in Table II. From Table II we can see that in lines #2, #3, #6, and #7 of the truth table Cout = Cin Therefore, in order to transfer the carry input to the carry output, it is enough to set A[i] =NOT B[i] The proposed scheme is based on this observation.

The implementation of the proposed weighted pattern generation scheme is based on the accumulator cell presented in Fig. 1, which consists of a Full Adder (FA) cell and a D-type flip-flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs. In Figure. 1, we assume, without loss of generality, that the set and reset are active high signals. In the same figure the respective cell of the driving register B[i] is also shown. For this accumulator cell, one out of three configurations can be utilized, as shown in Figure. 2.

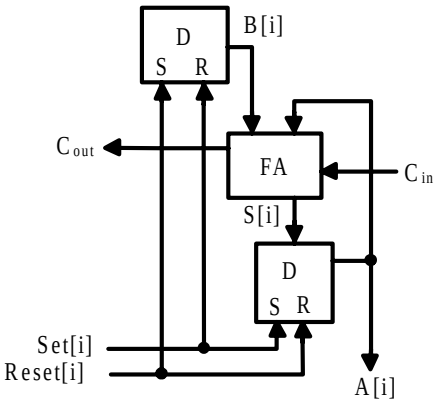

Fig 1 : *Accumulator cell.*

In Figure. 2(a) we present the configuration that drives the CUT inputs When A[i] = 1 is required Set[i] = 1 and Reset [i]= 0 and hence A[i] = 1 and B[i] = 0 Then the output is equal to 1, and Cin is transferred to $C_{out.}$

In Figure. 2(b) we present the configuration that drives the CUT inputs When A[i] = 0 is required Set[i] = 0 and Reset [i]= 1 and hence A[i] = 0 and B[i] = 1 Then the output is equal to 1, and Cin is transferred to $C_{out.}$

In Figure. 2(c), we present the configuration that drives the CUT inputs when A[i] = "-"is required Set[i] = 0 and Reset [i]= 0. The D input of the flip-flop of register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate satisfactorily random patterns to the inputs of the CUT.

In Figure. 3, the general configuration of the proposed scheme is presented. The Logic module provides the Set[n-1:0] and Reset[n-1:0] signals that drive the S and R inputs of the Register A and Register B inputs. Note that the signals that drive the S inputs of the flip-flops of Register A, also drive the R inputs of the flip-flops of Register B and vice versa. Figure. 2. Configurations of the accumulator cell of Figure. 1. Are represented in the following forms a, b and figure c as follows.

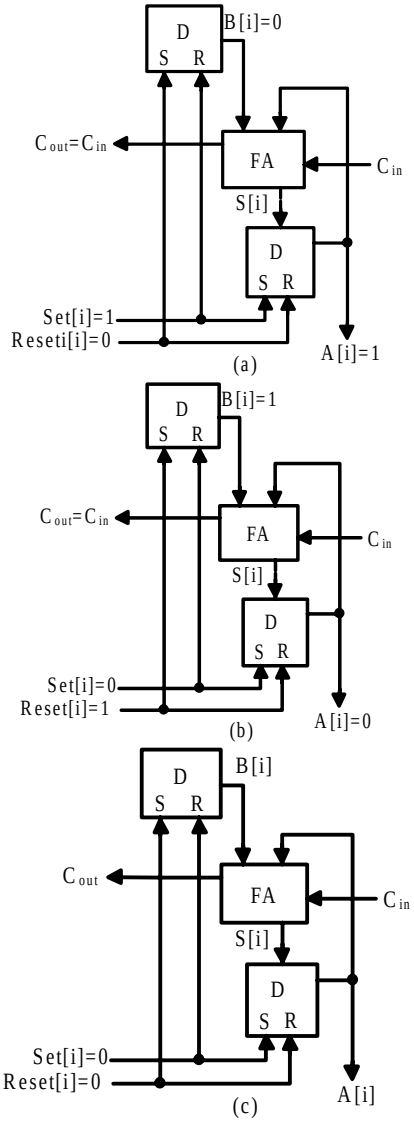

Fig. 2: *a ,b , c Configurations of the accumulator cell of Fig. 1.*

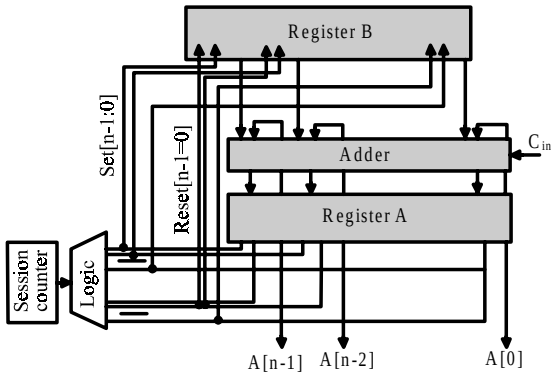

Fig. 3*: Proposed scheme*

IV. IMPLEMENTATION AND RESULTS

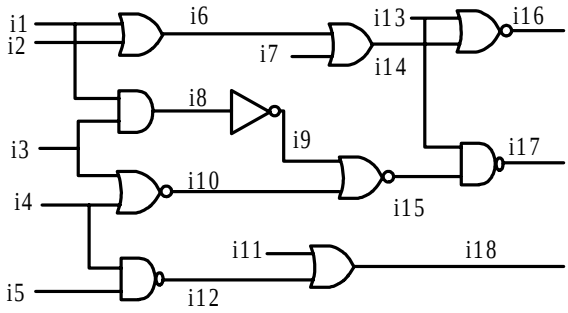

Figure 4 : *8-Input Circuit Design*

As we developed a circuit with different gates having 8 inputs and 3 outputs. As there are 18 nets we have used therefore 36 faults can be generated from these nets. As there are two types of faults will be produced. The faults are struck at 0 faults and struck at 1 fault. Different types of fault patterns are generated From this circuit . The controllability and observability of the faults should be observed. At each pattern different number of faults is covered.

	P1	P2	P3	P4
I1	1	x	0	0
I2	0	1	0	1
I3	0	0	x	1
I4	x	1	1	1
I5	1	1	x	x
I7	1	x	1	0
I11	0	x	1	x
I13	x	0	0	x

Table III : *Generated Patterns*

A Typical weight assignment procedure involves separating the patterns into 2 subsets:S1 and S2 as follows:S1={P1,P3}, and S2 = {P2,P4}.

The weight assignments for these subsets are W(S1)={-,0,0,1,1,1,-,0}, and W(S2) = {0,1,-,1,1,0,1,0} where "_" denotes the pseudorandom value,"1" denotes input is constantly driven by logic 1,"0" denotes input is constantly driven by logic 0.

	(P1,P3)	(P2,P4)
I1	0.5	0
I2	0	1
I3	0	0.5
I4	1	1
I5	1	1
I7	1	0
I11	0.5	1
I13	0	0

Table IV : *Subset Patterns With Weights*

The proposed system is implemented by using a test vector generator as shown in the figure and verilog code is implemented , and simulated. At different ns of time different patterns aregenerated. By using accumulator based3 weight pattern generation using LFSR all the patterns are efficiently generated.

The proposed Low hardware Accumulator Based 3-Weight Pattern Generation for Boundary Scan designed using Verilog hardware description language and structural form of coding. The proposed system simulation results are as follows

Simulation Results

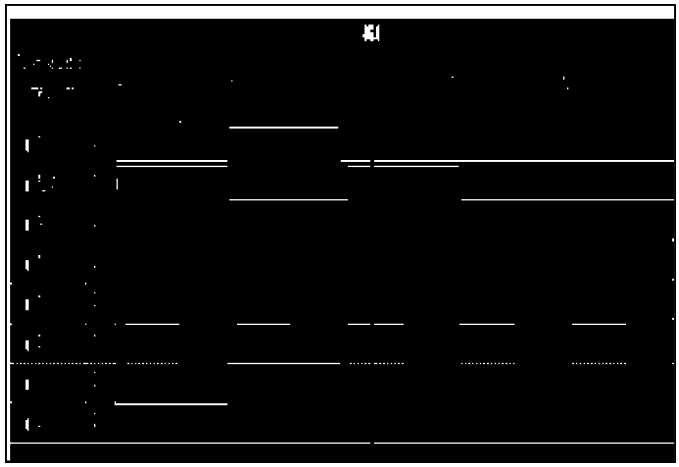

Figure.5 : *Result of accumulator cell*

when si = 1 ri = 0 ,and ai = 0 is required then we will get the cy = 0 that will be transferred to the output and a_out = 1.when si = 0 , ri = 1 , and ai = 1 is required then we will get the cy = 1 that will be transferred to the output and a_out = 0 when si = 0 , ri = 0 , and ai = 0 is required then we will get the cy = 0 that will be transferred to the output and a_out = 1

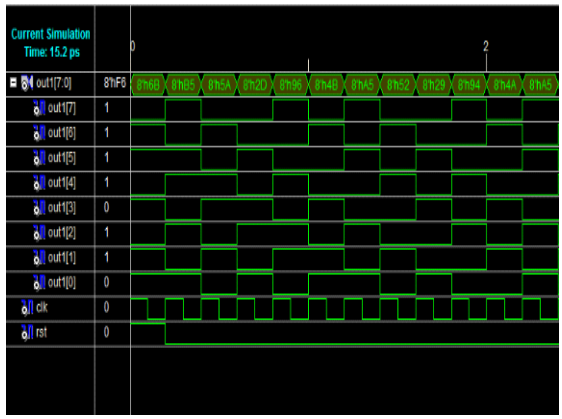

Figure.6 *Result of 3 weighted pattern generation*

The proposed system contains of season counter and lfsr (linear feedback shift register). Which is used to produce internal signals for the different combinations . it produces different combinations of test patterns for given any circuit.

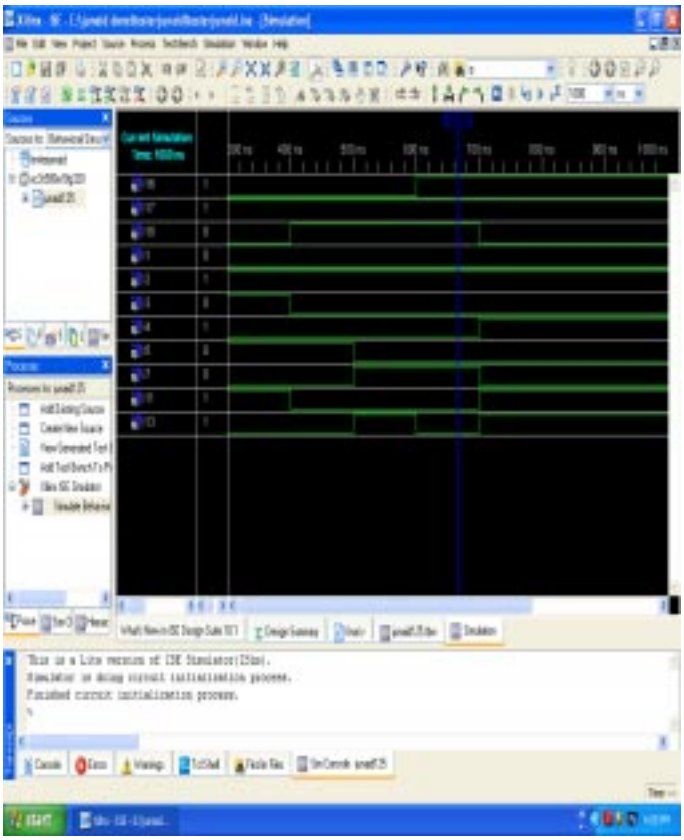

Figure 7 : *3-Weight BIST*

The above result shows that by taking only 8 signals as external inputs and with different combinations of gates gives a inner circuits which produces three 3 output signals as i16, i17, i18. By connecting the proposed design circuit output to the inner circuit i.e. shown in **Figure 4**: 8-Input Circuit Design we can check the weather generated output test patterns are correct or not. So we can avoid the faults and fault coverage will be maximum.

Circuit	Hardware iverhead		
Name	[11]	Prop	Decr.
C1355	28%	5%	81%
C3540	11%	4%	63%
C7552	17%	4%	76%

Table V : *comparison of hardware*

V. CONCLUSION

The proposed system is an accumulator-based 3-weight (0, 0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns and connected with inner circuits that check the output value to avoid the faults. Comparisons with a previously proposed accumulator-based3-weight pattern generation technique indicate that the hardware overhead of the proposed scheme is lower while at the same time this weighted pattern generation with accumulator covers all the patterns and the test time is also less. The test patterns are generated automatically for applied test vectors so that there is 100% fault coverage. Comparisons with scan based schemes show that the proposed schemes results in lower hardware overhead. Finally, comparisons with the accumulator- based scheme proposed reveal that the proposed scheme results in significant decrease in hardware overhead

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Indexa Novel Approach For Enhancement of Contrast and Sharpness of an Image

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ABSTRACT

In the applications like medical radiography enhancing movie features and observing the planets it is necessary to enhance the contrast and sharpness of an image. We propose a generalized unsharp masking algorithm using the exploratory data model as a unified framework. The proposed algorithm is designed to address three issues:1) simultaneously enhancing contrast and sharpness by means of individual treatment of the model component and the residual,2)reducing the halo effect by means of an edge-preserving filter, and 3)solving the out of range problem by means of log ratio and tangent operations. We present a new system called the tangent system which is based upon a specific bregman divergence. Experimental results show that the proposed algorithm is able to significantly improve the contrast and sharpness of an image. Using this algorithm user can adjust the two parameters the contrast and sharpness to have desired output

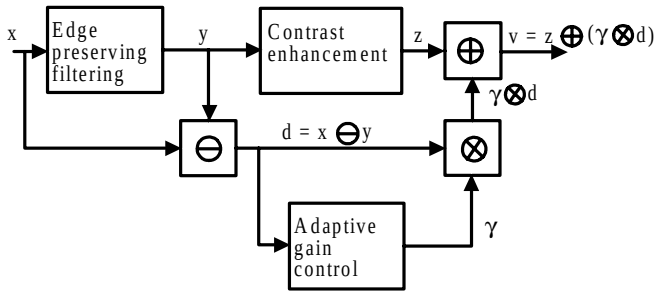
Index Terms

Bregman divergence, exploratory data model, generalized linear system, image enhancement, unsharp masking.

I. INTRODUCTION

Now a days in digital image processing applications requires an image that contains detailed information. So we need to convert a blurry image and undefined image into a sharper image. So in application orientation we need to enhance the contrast and sharpness of the image. While enhancing the qualities of the image, it is clear that noise components enhancement is undesirable. In this view the enhancement of undershoot and overshoot creates the effect called as halo effect. So ideally our algorithm should only enhance the image details. To overcome this problem we need to use filters that are not sensitive to noise and do not smooth sharp edges. In this paper we use log ratio approach to overcome the out of range problem.

In this paper we proposed a generalized system which is used for general addition and multiplication which is shown in below figure.



$$x \oplus y = \phi^{-1}[\phi(x) + \phi(y)] \quad \text{.....(1)}$$

and $$\alpha \otimes x = \phi^{-1}[\alpha\phi(x)] \quad \text{.....(2)}$$

Where x and y are sample signals, α is a real scalar and ø is non-linear function. And the remarkable property of log ratio approach is that it is operable in the region (0, 1) gray scale and can overcome the out of range problem. The following are the main issues in contrast enhancement and sharpness enhancement in current existing systems. The existing systems dealt these processes as two tasks which will increase the complexity. The contrast enhancement does not lead to the sharpness enhancement. Many of the existing systems facing the

problem of halo effect. While enhancing the sharpness of an image, in parallel the noise of the image also is increased. Though all the systems have enhanced the sharpness and contrast of the image, this will give the best result only after careful rescaling process. This was not there in existing system. These issues can be solved through our approach using exploratory data model and log ratio approach.

II. EXPLORATORY DATA ANALYSIS MODEL FOR IMAGE ENHANCEMENT

A well known idea in exploratory data analysis is to decompose a signal into two parts. From This point of view, the output of the filtering process, denoted y = f(x), can be regarded as the part of the image that fits the Model. Thus,

$$x = y \oplus d \qquad \text{.....(3)}$$

Where d is called as detail signal (the residual) and defined as $d = x \ominus y$ where θ is generalized subtraction. The general form of unshaped masking algorithm is as follows.

$$V = h(y) \oplus g(d) \qquad \text{.....(4)}$$

Where v is the output and h(y) and g(d) are the linear or non-linear functions. Explicitly we can say that the image model that is being sharpened is the residual. In addition, this model permits the incorporation of contrast enhancement by means of a suitable processing function h(y) such as adaptive histogram equalization. As such, the generalized algorithm can enhance the overall contrast and sharpness of the image.

Figure 2. Generalized unsharp masking algorithm block diagram

The following is the comparison between classical unsharp masking algorithm and generalized unsharp masking algorithm.

	y	d	h(y)	g(d)	Output v	Re-scale
UM	LPF	x-y	Y	γd	y+g(d)	Yes
GUM	EPF	$x \ominus y$	ACE	$\gamma(d) \otimes d$	h(y) $\oplus$ g(d)	No

We address the issue of the halo effect by using an edge-preserving filter-the IMF to generate the signal. The choice of the IMF is due to its relative simplicity and well studied properties such as the root signals. We address the issue of the need for a careful rescaling process by using new operations defined according to the log-ratio and new generalized linear system. Since the gray scale set is closed under these new operations

We address the issue of contrast enhancement and sharpening by using two different processes. The image y is processed by adaptive histogram equalization and the output is called h(y). The detail image is processed by $g(d) = \gamma(d) \otimes d$ where $\gamma(d)$ is the adaptive gain and is a function of the amplitude of the detail signal d. The final output of the algorithm is then given by

$$v = h(y) \oplus [\gamma(d) \otimes d] \qquad \text{.....(5)}$$

III. LOG-RATIO, GENERALIZED LINEAR SYSTEMS AND BREGMAN DIVERGENCE

The new generalized operations will be defined using the equations (1) and (2). Here these operations are defined based on the view vector space used logarithmic image processing.

A. definitions and properties of log-ratio operations

Nonlinear Function: We consider the pixel gray scale $x \in (0,1)$ of an image. For an N-bit image, we can first add a very small positive constant to the pixel gray value then scale it by 2^{-N} such that it is in the range (0, 1). The nonlinear function is defined as follows:

$$\phi(x) = \log \frac{(1-x)}{x} \qquad \text{.....(6)}$$

To simplify notation, we define the ratio of the negative image to the original image as follows:

$$X = \varphi(x) \frac{1-x}{x} \qquad \text{.....(7)}$$

Using equation (1) the addition of two gray scales x_1 and x_2 can be defined as

$$x_1 \oplus x_2 = \frac{1}{(1+\varphi 1(x)\phi = \varphi 2(x))} = \frac{1}{1+x1x2} \qquad \text{.....(8)}$$

And the multiplication of the gray scale x by a real scalar α $(-\infty < \alpha < +\infty)$ is defined using (2) as follows

$$\alpha \otimes x = \frac{1}{1+X^{\alpha}} \qquad \text{.....(9)}$$

This operation is called as scalar multiplication and we define a new zero scale denoted by e as follows

$$e \otimes x = x \qquad \text{.....(10)}$$

The value of $|x|$ can be defined as follows.

$$|x| = \begin{cases} x, & 1/2 \le x < 1 \\ 1-x & 0 \le x < 1/2 \end{cases} \qquad \text{.....(11)}$$

Negative image and subtraction operation:

The negative of the gray scale, denoted by, is obtained by solving

$$x \oplus \bar{x} = 1/2 \qquad \text{.....(12)}$$

Now we can define the subtraction operation using the addition operation defined in (8) as follows.

$$x_1 - x_2 = x_1 \oplus (\theta x_2)$$
$$= \frac{1}{1+\varphi(x_1)\varphi(x_2)}$$
$$= \frac{1}{(1+x_1 x_2^{-1})} \qquad \text{.....(13)}$$

Properties :

Now when positive value a is added to the gray scale x then there will be fluctuations in output image y based on the values of a given below.

Order of reflections of the log-ratio addition.

$0 < a < 1/2$	$1/2 < a < 1$	
$0 < x < 1/2$	$0 < x \oplus a < \min(x,a)$	$x < x \oplus a < a$
$1/2 < x < 1$	$a < x \oplus a < x$	

Order of reflections of the log-ratio multiplication.

$0 < \alpha 1$	$\alpha > 1$	
$0 < x < ½$	$0 < \alpha 1$	$\alpha \otimes x < x$
$1/2 < x < 1$	$\alpha \otimes x < x$	$\alpha \otimes x > x$

In case of log-ratio addition, based on the value of the constant 'a' the variation of output gray value y is shown in the above table. The variations in y depends on the positive and negative nature of the gray scale x and the constant 'a'. While coming to log-ratio multiplication the result will be based on the gain value α and the polarity of the gray scale x.

Computation:

Computations can be directly performed using the new operations. For example, for any real numbers α_1 and α_2, the weighted summation is given by

$$(\alpha_1 \otimes x_1) \oplus (\alpha_2 \otimes x_2) = \frac{1}{1 + x_1^{\alpha_1} x_2^{\alpha_2}} \qquad \text{.....(14)}$$

the generalized weighted averaging operation is defined as

$$y = (\alpha_1 \otimes x_1) \oplus (\alpha_2 \otimes x_2) \oplus (\alpha_3 \otimes x_3) \ldots . \oplus (\alpha_n \otimes x_n)$$
$$= \frac{G}{\bar{G} + G} \qquad \text{.....(15)}$$

Where $G = \left(\Pi x_n^{a_n}\right)^{1/N}$ and $\bar{G} = \left(\Pi (1 - x_n)^{a_n}\right)^{1/N}$ are the weighted geometric means of the original and the negative images, respectively.

An indirect computational method is through the nonlinear function (6).

$$y = \phi^{-1}\{\phi[(\alpha_1 \otimes x_1) \oplus (\alpha_2 \otimes x_2 \oplus \quad \ldots . (\alpha_n \otimes x_n))]\} \qquad \text{.....(16)}$$

B. Log-Ratio, the Generalized Linear System and the Bregman Divergence:

We study the connection between the log-ratio and the Bregman divergence.

1) Log-Ratio and the Bregman divergence:

The Bregman divergence of two vectors x and y, denoted $D_F(X \| Y)$ is defined as follows:

$$D_F(X \| Y) = F(Y) - (X - Y)^T \nabla F(Y) \qquad \text{.....(17)}$$

Where $F : N \to R$ a strictly convex and differentiable function defined over an open convex domain N and ∇F is the gradient of F evaluated at point y. the weighted left-sided centroid is given by

$$C_L = \arg\min_{c \in N} \sum_{n=1}^{N} \alpha_n D_F(C \| X_n)$$
$$\nabla F^{-1}\left(\sum_{n=1}^{N} \alpha_n \nabla F(X_n)\right) \qquad \text{.....(18)}$$

Comparing equations (17) and (19) we can see that x_n is scalar and we can conclude as follows.

$$F(x) = \int \phi(x) dx$$
$$= -x \log(x) - (1-x)\log(1-x) \qquad \text{.....(19)}$$

Where the constant of the indefinite integral is omitted. The previous function F(x) is called the bit entropy and the corresponding Bregman divergence is defined as

$$D_F(x \| y) = -x \log\left(\frac{x}{y}\right) - (1-x)\log(1-x)/(1-y) \qquad \text{.....(20)}$$

This is called as logistic loss. Therefore, the log-ratio has an intrinsic connection with the Bregman divergence through the generalized weighted average. This connection reveals a geometrical property of the log-ratio which uses a particular Bregman divergence to measure the generalized distance between two points. This can be compared with the classical weighted average which uses the Euclidean distance. In terms of the loss function, while the log-ratio approach uses the logistic loss function, the classical weighted average uses the squared loss function.

2) Generalized Linear Systems and the Bregman Divergence:

we can derive the connections between the bregman divergence with other established generalized linear

systems such as the MHS with $\phi(s)=\log(x)$ where $x\in(0,\infty)$ and the LIP model $\phi(x)=-\log(1-x)$ Type equation here. where $x\in(-\infty,1)$ the corresponding bregman divergences are the kullback-Leibler(KL) for MHS

$$D_F(x,y)=x\log\left(\frac{x}{y}\right)-(x-y) \qquad .....(21)$$

And the LIP

$$D_F(x,y)=(1-x)\log[(1-x)/(1-y)]-[(1-x)-(1-y)] \qquad .....(22)$$

Respectively.

3) A new generalized system:

We can define a new generalized system by letting $\phi(x)=\nabla F(x)$. This approach of defining a generalized linear system is based upon using the Bregman divergence as a measure of the distance of two signal samples. The measure can be related to the geometrical properties of the signal space. A new generalized linear system for solving the out-of-range problem can be developed by using the following Bregman divergence

$$D_F(X,Y)=\frac{1-xy}{1-y^2}-\sqrt{1-x^2} \qquad .....(23)$$

Which is generated by the convex function $F(x)=-\sqrt{(1-x^2)}$ whose domain is (1,-1). The nonlinear unction or $\phi(x)$ the corresponding generalized linear system is as follows: $\phi(x)=\frac{dF(x)}{dx}=\frac{x}{\sqrt{1-x^2}}$ (24)

In this paper the generalized system is called as tangent system and the scalar addition and multiplication (equation (1) and (2)) is called as tangent operations.

In image processing applications the pixel values from the interval $[0,2^N)$ is mapped into (1,-1).then the image is processed using tangent operations and then the image is mapped to $[0,2^N)$ as reversible operation. The total signal set is confined to (-1,1) and hence using this the out-of –range problem can overcome using log-ratio. We can define the negative image and the subtraction operation, and study the order relations for the tangent operations.

IV. PROPOSED ALGORITHM

A. Dealing with Color Images

We first convert a color image from the RGB color space to the HSI or the LAB color space. The chrominance components such as the H and S components are not processed. After the luminance component is processed, the inverse conversion is performed. An enhanced color image in its RGB color space is obtained. The rationale for only processing the luminance component is to avoid a potential problem of altering the white balance of the image when the RGB components are processed individually.

B. Enhancement of the Detail Signal

1) The Root Signal and the Detail Signal : Let us denote the Median filtering operation as a function $y=f(x)$ which maps the input to the output. An IMF operation can be represented as: $y_{k+1}=f(y_k)$ where $k=0,1,2,3.....$ is the iteration index and $y_0=x$ .The signal y_n is usually called the root signal of the filtering process if $y_{n+1}=y_n$ .It is convenient to define the root signal as follows.

$$n=\min k, \qquad \text{subject to } H(y_k,y_{k+1})<\delta$$

Where $H(y_k,y_{k+1})$ is the suitable measure between the two images and δ is a user defined threshold.

It can be easily seen that the definition of the root signal depends upon the threshold.

2) Adaptive Gain Control

We can see from Figure. 3 that to enhance the detail signal the gain must be greater than one. Using a universal gain for the whole image does not lead to good results, because to enhance the small details a relatively large gain is required. However, a large gain can lead to the saturation of the detailed signal whose values are larger than a certain threshold. Saturation is undesirable because different amplitudes of the detail signal are mapped to the same amplitude of either 1 or 0.This leads to loss of information. Therefore, the gain must be adaptively controlled. In the following, we only describe the gain control algorithm for using with the log-ratio operations. Similar algorithm can be easily developed for using with the tangent operations.

To Control the gain; we first perform a linear mapping of the detail signal d to a new signal c

$$c = 2d - 1 \qquad .....(30)$$

Such that the dynamic range of c is (-1, 1). A simple idea is to set the gain as a function of the signal c and to gradually decrease the gain from its maximum value γ_{MAX} when $|x<T$ to its minimum γ_{MIN} value when

$|c| \to 1$.More specifically, we propose the following adaptive gain control function

$$\gamma(c) = \alpha + \beta \exp\left(-|c|^{\eta}\right) \quad \text{.....(31)}$$

Where η is a parameter that controls the rate of decreasing. The two parameters α and β are obtained by solving the equations:

$\gamma(0) = \gamma(1) = Y_{MIN}$. For a fixed η, we can easily determine the two parameters as follows:

$$\beta = (\gamma_{MAX} - \gamma_{MIN}) / \left(1 - e^{-1}\right) \quad \text{.....(32)}$$

and $\alpha = \gamma_{MAX} - \beta$

Although both γ_{MAX} and γ_{MIN} could be chosen based upon each individual image processing task, in general it is reasonable to set $\gamma_{MIN} = 1$.This setting follows the intuition that when the amplitude of the detailed signal is large enough, it does not need further amplification. For example, we can see that

$$\lim_{|d|_o \to 1} \gamma \otimes d = \lim_{|d|_o \to 1} \frac{1}{(1+\gamma)(1-d)/d} = 1 \quad \text{.....(34)}$$

As such, the scalar multiplication has little effect. We now study the effect of γ and γ_{MAX} by setting $\gamma_{MIN} = 1$.

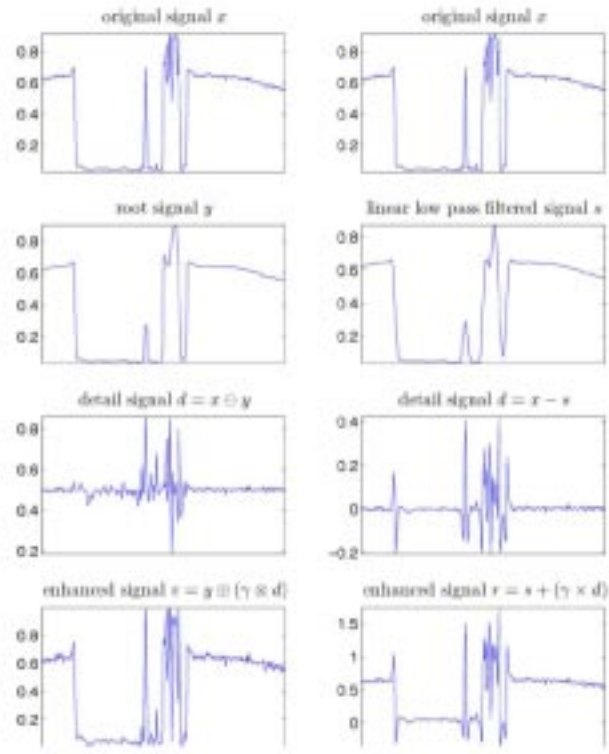
C. Contrast Enhancement of the Root Signal

For contrast enhancement, we use adaptive histogram equalization implemented by a Matlab function in the Image Processing Toolbox. The function, called "adapthisteq," has a parameter controlling the contrast. This parameter is determined by the user through experiments to obtain the most visually pleasing result. In our simulations, we use default values for other parameters of the function.

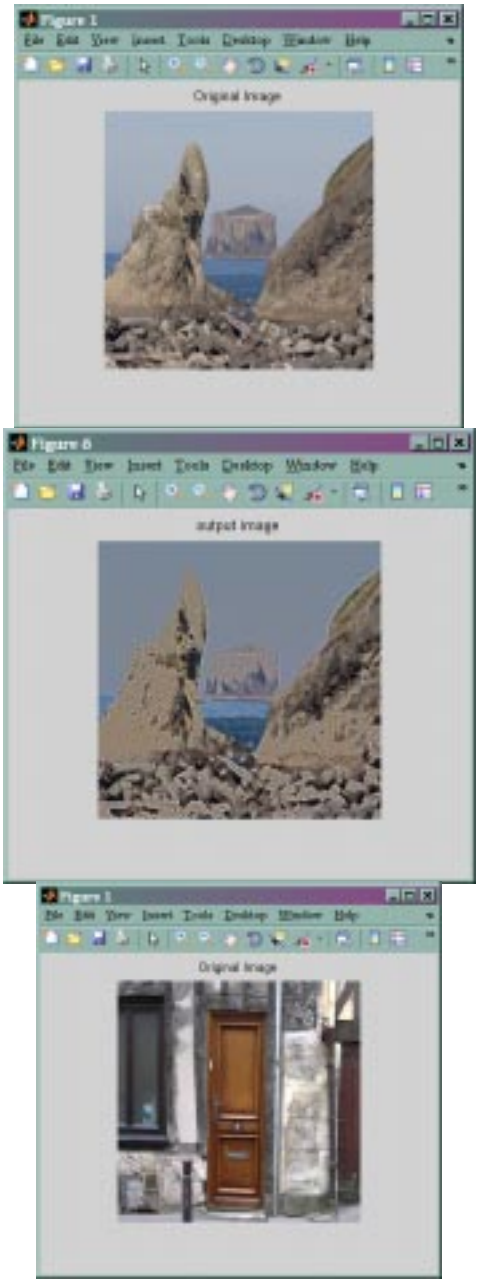
V. RESULTS AND COMPARISON

We first show the effects of the two contributing parts: contrast enhancement and detail enhancement. Contrast enhancement by adaptive

Histogram equalization does remove the haze-like effect of the original image and contrast of the cloud is also greatly enhanced. Next, we study the impact of the shape of the filter mask of the median filter. For comparison we also show the result of replacing the median filter with a linear filter having a uniform mask. As we can observe from these results, the use of a linear filter leads to the halo effect which appears as a bright line surrounding the relatively dark mountains (for Using a median filter, the halo effect is mostly avoided, although for the square and diagonal cross mask there are still a number of spots with very mild halo effects. However, the result from the horizontal-vertical cross mask is almost free of any halo effect. In order to completely remove the halo effect, adaptive filter mask selection could be implemented: the horizontal- vertical cross mask for strong vertical/horizontal edge, the diagonal cross mask for strong diagonal edge and the square mask for the rest of the image. However, in practical application, it may be sufficient to use a fixed mask for the whole image to reduce the computational time. We have also performed experiments by replacing the log ratio operations with the tangent operations and keeping the same parameter settings. We observed that there is no visually significant difference between the results.



The above shown graphs are the main differnces between the classical and generalized unsharp masking algorithm. Here we show the clear difference between the addition and generalized addition. And at last we show that the enhancement is more in generalized unsharp masking algorithm rather than in classical unsharp masking algorithm.



The above are the two results which processed using generalized unsharp masking algorithm. These two output images show that the sharpness and contrast get enhanced in an exponential manner. No rescaling process is used here. And the out of range problem is not encountered here since the range of gray scale is (0, 1).

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Reducing the Complexity of FIR Filters By Using Prototype and Masking Filters Splitting With FRM

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ABSTRACT

The main objective of this paper is to design multi-channel, non-uniform fini impulse response filter with sharp transition band and low complexity. For this, FIR filter using frequency response masking has to be designed. Multi-channel non-uniform FIR filter bank is to be designed by the Frequency Response Masking (FRM) filters. The complexity of these multi-channel FRM filter bank is reduced by using reconfigurable filter bank architecture. The complexity is further reduced by using multi stage reconfigurable architecture. In this multi-stage reconfigurable architecture method multi-stage masking filter splitting and multi-stage prototype filter splitting is done for generalization.

Keywords

Fir filters, interpolation,decimation, frequency response masking,reconfigurable filterbank

I. INTRODUCTION

Digital signal processing techniques are being applied to wireless communication systems, digital TVs, and multimedia systems. which have resulted in a demand for narrow transition-width FIR digital filters. A major drawback for the FIR filter is the large number of arithmetic operations needed to get narrow transition-width. Therefore it is necessary to study different available techniques to reduce the transition width of the filter with reduced complexity. One of the most successful techniques for synthesis of very narrow transition width FIR filter with very low complexity is the frequency response masking technique (FRM) [1].

The Frequency Response Masking (FRM) FIR filters design technique gives sharp transition band by employing low order digital sub filters. The constituent digital sub filters are designed by using Parks McClellan approach [2]. These FIR filters based on FRM (frequency response masking) can be used in uniform and non-uniform filter banks and the performance of filter banks can be studied.

In a Software Defined Radio (SDR) receiver, the specifications of the channelizer changes as the mode of communication changes. In conventional multi-mode channelizers a separate channelizer is needed for each mode/channel. Conventional FRM based channelizers is not an efficient approach due to its increased hardware complexity and poor resource utilization. In the reconfigurable FRM filter bank based channelizers, a reconfigurable architecture is used instead of using separate channelizer for each mode. In this method, same prototype filter is used to design separate channels. [4]

II. REVIEW OF FRM APPROACH

The basic structure of FRM filter is as shown below

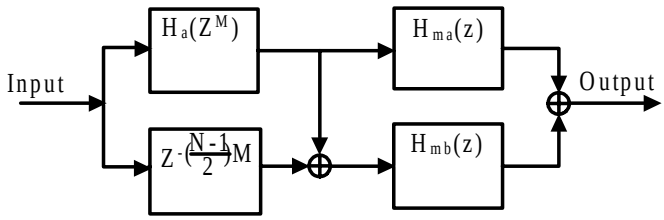

Figure1 : *Basic structure of FRM filter*

Let $H(z)$ be the desired FRM FIR low pass digital filter with pass band edge frequency of f_p and stop band edge frequency of f_s and $H_a(z)$ be the transfer function of a linear phase low pass FIR band edge shaping filter with a passband edge frequency of f_{ap} and a stopband edge frequency of f_{as} If $H_b(z)$ represents complementary filters of $H_b(z)$,

Then,

$$H_b(z) = z^{-\left(\frac{N-1}{z}\right)} - H_a(z) \quad \text{.....(1)}$$

We can obtain $H_a(z^M)$ and (z^M) by interpolating $H_a(z)$ and $H_b(z)$ respectively with interpolation factor M. The desired FRM FIR digital filter transfer function can be realized as shown below

$$H(z) = H_a(z^M)H_{ma}(z) + H_b(z^M)H_{mb}(z) \quad \text{.....(2)}$$

Where $H_{ma}(z)$ and $H_{mb}(z)$ represents the masking digital sub filters. Then the transition width of the resulting FIR digital filter H (z) is scaled transition width of

$$H(z) = \frac{f_{as} - f_{ap}}{M}.$$

Design Equations

To design the prototype filter $H_a(z)$, the pass band and stop band edge frequency specifications f_{ap} and f_{as} are

$$f_{ap} = f_p M - m \text{ , } f_{as} = f_s M - m \quad \text{.....(3)}$$

Here f_p and f_s are pass band and stop band edge specifications of H (z).m is the largest integer less than $f_p M$, i.e, $m <= \lfloor f_p M \rfloor$ .M is interpolation factor value. To design these masking and masking complementary filters the desired specifications f_{map} , f_{mas}, f_{mbp} and f_{mbs} are

$$f_{map} = f_p \text{ , } f_{mas} = \frac{m+1-f_{as}}{M}, \; f_{mbp} = \frac{m-f_{ap}}{M} \text{ and } f_{mbs} = f_s \quad \text{.....(4)}$$

Frequency response illustration of Frequency Response masking approach

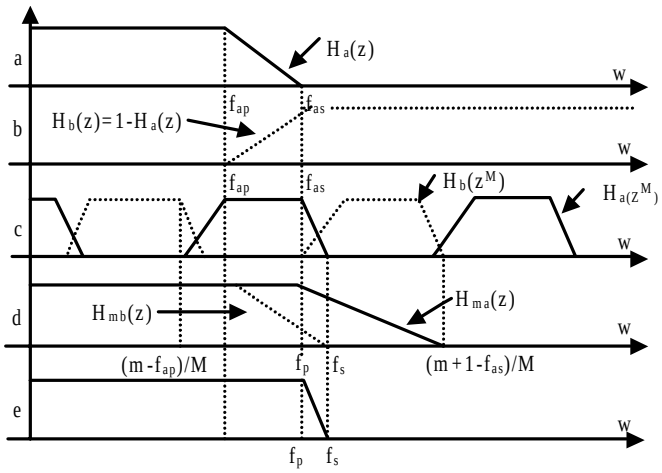

Figure 2 : *Frequency response illustration of Frequency Response masking approach [1]*

III. MULTI STAGE FRM FILTER DESIGNS

In multi-stage frequency response masking filter design technique [1], if the prototype filter order is high, it may be implemented as a system of sub filters using the frequency-response masking technique. Thus the complexity of prototype filters and hence the complexity of the overall filter architecture will be reduced.

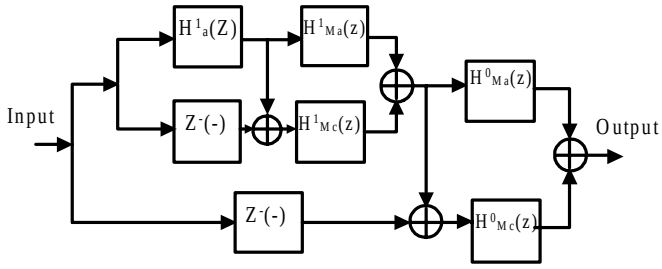

Figure3 : *Multi-stage frequency response masking filter*

IV. RECONFIGURABLE MULTI-CHANNEL MULTI-STAGE FRM FILTER BANK

In reconfigurable single stage multi-channel frequency response masking filter bank, if the interpolation factor is high, the order and hence the complexity of the masking filter becomes high. We can reduce the order and complexity of masking filters by using reconfigurable multi stage multi masking. The architecture of two-stage two-channel FRM filter bank is shown below. In this example first channel masking filter is implemented in two stages.

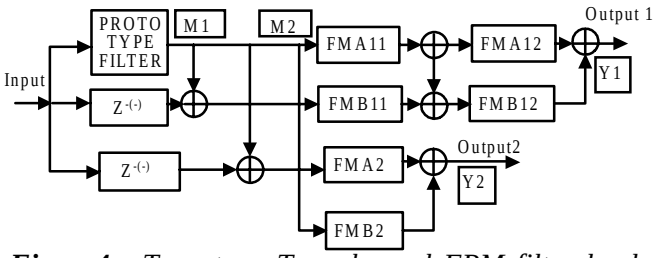

Figure4 : *Two-stage Two channel FRM filter bank*

Here FMA11 and FMB11 are the masking and masking complementary filters of first channel first stage FMA12 and FMB12 are the masking and masking complementary filters of first channel second stage. FMA2 and FMB2 are the masking and masking complementary filters of second channel first stage.

V. GENERALISED RECONFIGURABLE FILTER BANK

In this method we will do both splitting of prototype filter by using another frequency response masking filter and splitting of masking filters by using masking filter splitting method. This method is called generalized reconfigurable filter bank method. By using this method we can get multi-channels for multi-stages with reduced complexity. The

design steps for generalized method is given below

For an n-channel filter bank.

Let $f_{p1}, f_{p2}, ..., f_{pn}$ are the pass band frequencies and $f_{s1}, f_{s2}, ..., f_{sn}$ are the stop band frequencies of the channels corresponding to different modes of operation.

1. Find the common prototype filter specifications f_{ap} and f_{as} for different channels by using below equations

$$f_{ap} = f_{p1}M_1 - \lfloor f_{p1}M_1 \rfloor = - - - - = f_{pn}M_n - \lfloor f_{pn}M_n \rfloor \quad .....(5)$$

$$f_{as} = f_{s1}M_1 - \lfloor f_{sa}M_1 \rfloor = - - - - - - = f_{sn}M_n - \lfloor f_{sn}M_n \rfloor .....(6)$$

By varying different interpolation factors we will get common prototype filter specifications with different interpolation factors.

2. After getting common prototype filter specifications we know the specifications of required filters and different interpolation factors, we will design the masking and masking filters by using these design equations

$$m = \lfloor f_p M \rfloor, f_{map} = f_p, f_{mas} = \frac{(m+1) - f_{as}}{M}$$

$$f_{mcp} = \frac{m - f_{ap}}{M} \text{ and } f_{mcs} = f_s \quad .....(7)$$

3. After getting masking and masking complementary filters, calculate the length of prototype filter by using below equation

$$N = \frac{-2\log_2(10\delta_1\delta_2)}{3(\nabla\omega)} - 1 \quad .....(8)$$

Where δp and δs are the peak pass band and stop band ripples respectively.

4. Now we will compare the orders of prototype, masking and masking complementary filters N_a, N_{ma}, N_{mb} for diff channels

If $N_a >> N_{ma}$ and N_{mb} we will use multi-stage prototype filter method

5. To implement multi-stage prototype filter
   a. Calculate the length of the prototype filter.
   b. If $N_{prototype} >> N_{masking}$, then split prototype filter by using another FRM instead of on FIR filter.
   c. Check whether $N_{prototype} <= N_{masking}$, for all the stages.If the condition is not satisfied proceed to further splitting of prototype filter until $N_{prototype} <= N_{masking}$ or until further factorization cannot be done.
6. To implement multi-stage masking filter
   a. Calculate the length of the masking filter.
   b. If $N_{masking} >> N_{prototype}$, then factorize M into two factors $M = M_i, M_j$.
   c. Check whether $N_{masking} << N_{prototype}$, for all the factorized M values. If the condition is not satisfied proceed to further factorize M_i or M_j until $N_{masking} < N_{prototype}$ or until further factorization cannot be done.

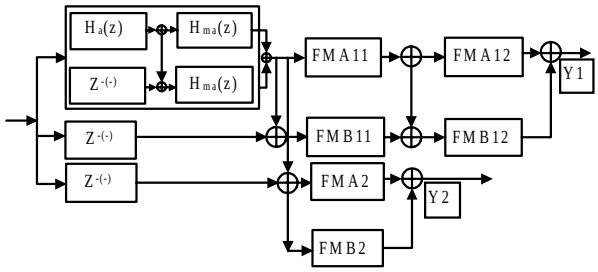

Figure5 : *Generalized method*

VI. A DESIGN EXAMPLE

The design example is presented here to compares the proposed method with multi-channel multi-stage reconfigurable filter bank method. For two-channel filter bank, required filter specifications of first channel and second channels are, pass-band and stop-band edges are 3000KHz and 3010 KHz and 12500KHz and 12510 KHz respectively. The peak pass-band ripple and peak stop-band ripple specifications for two channels are chosen as 0.1dB and -40dB respectively [6]

For these required filter specification we need to find out common prototype filter specifications by using equation(5) & (6). After getting common prototype filter specification we will design prototype filter with common filter specifications f_{ap} and f_{as}. Now we have the required filter specifications

$f_{p1} = 3000, f_{s1} = 3010, f_{p2} = 12500$ and $f_{s2} = 12510$.

Substituting these values in equation (5) and (6) we obtain two different interpolation factors $M_1 = 25$ and $M_2 = 6$.

Now we know required filters specifications and interpolation factors and we can design masking and masking complementary filter specifications by using basic

FRM design specifications. In this example we got the prototype filter order 391 by using expression

$$N = \frac{-2\log_2(10\delta_1\delta_2)}{3(\nabla\omega)} - 1 \qquad \text{.....(9)}$$

and masking filters orders for first channel and second channel are 29 and 42 respectively. Here compare to prototype filter, masking and masking complementary filter orders are less so instead of one prototype filter we are going for another frequency response masking filter. After inserting another frequency response masking filter the orders of that filter are 213+23+23 is 259.

So comparison is explained in next section

In the below figure

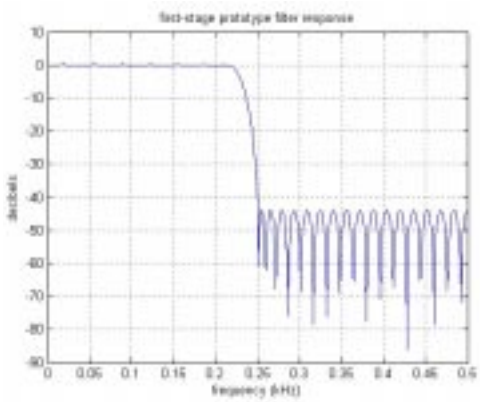

Figure6 (a) : *First stage prototype filter response*

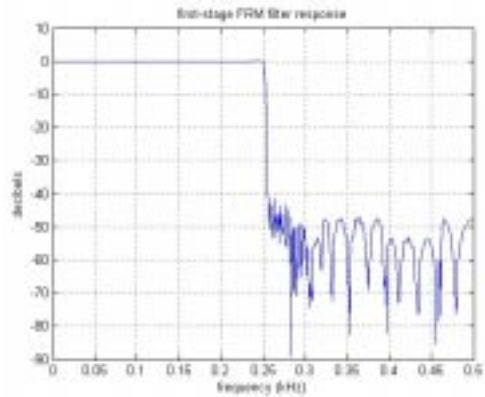

Figure6 (b) : *First-stage FRM response*

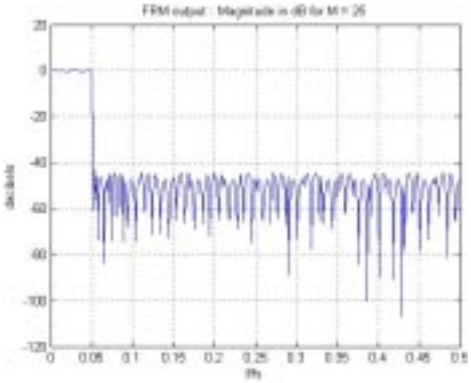

Figure6(c) : *First channel FRM response*

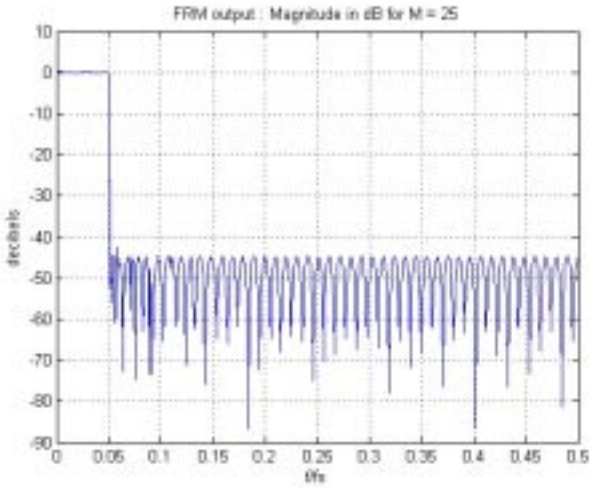

Figure6(d) : *Second channel FRM Response*

VII. COMPLEXITY COMPARISION

To compare filters we need number of multipliers used to design particular filter. To find the multipliers in frequency response masking filter is

$$f(N) = \frac{N+1}{2} \quad \text{if N is odd}$$

$$\frac{N}{2} + 1 \quad \text{If N is even} \qquad \text{.....(10)}$$

$f(N)$ denotes the total no.of multipliers needed for the implementation of an FIR filter with order N.

I COMPLEXITY COMPARISION TABLE

	METHOD	N_a	N_{ma}	N_{mb}	N
1	Reconfigurable two-channel two-stage method	391	29	42	462
2	Proto type filter splitting method	259	20	19	298

In the above table N_a is the order of the prototype or model filter $H_a(z)$, N_{ma} is the order of the masking filter $H_{ma}(z)$,and N_{mc} is the order of the masking complementary filter $H_{mb}(z)$.

Also,

$$\prod = f(N_a) + f(N_{ma})f(N_{mb}) \qquad \text{.....(11)}$$

$\prod$ indicates the number of multiplications required to implement the overall filter. The overall filter order

$$N = N_a + N_{ma} + N_{mb} \qquad \text{.....(12)}$$

is N respectively to different channels.

From the above complexity comparison table for Reconfigurable two-channel two-stage method required

462 multipliers, but Reconfigurable two-channel two-stage with Proto type filter splitting method requires 298 multipliers. Reconfigurable two-channel two-stage method with Proto type filter splitting method is giving 64% multiplier saving compare to Reconfigurable two-channel two-stage method required.

VIII. CONCLUSION

The existing architecture with low power, low complexity and reconfigurability for software defined radio is modified in this paper. The prototype filter in the FRM structure is replaced by another FRM structure. Thus we get multiple channel architecture with very low complexity and low power which is ready for hardware implementation. This leads to the implementation of low power, low complexity multiplier-less, reconfigurable, non-uniform channel filters. Since different channels correspond to different communication standards, different objective functions and different optimization techniques may be used which may lead to better performance. Also this architecture can be extended to more number of channels.

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The Hardware Implementation of Motion Object Detection Based on Background Subtraction

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ABSTRACT

Currently, the market requires applications based on image and video processing with several real time constraints. Identifying the moving objects from a video sequence is the fundamental and critical task in robotics, surveillance and many computer vision applications. The commonly used technique is the background subtraction algorithm. There are many challenges in developing a good Background Subtraction algorithm. First, it should be robust to the changes in illumination. Second, it should avoid detecting non stationary objects like papers and shadows. This paper presents a new algorithm to detect moving objects with in a scene acquired by a stationary camera the output data provide a scene characterization allowing a simple and efficient pixel-change detection framework. This yields a good trade-off in terms of robustness and accuracy, with a minimal cost in memory and a low computational complexity. In this paper, a video surveillance-based image processing system is developed on Xilinx Spartan3 Field Programmable Gate Array (FPGA) device using embedded development kit (EDK) tools from Xilinx.

Keywords

video surveillance, FPGA, EDK, Micro Blaze, FSL Introduction

I. INTRODUCTION

Many embedded DSP systems make use of a DSP chip utilizing a single processing core with high-bandwidth memory connections to implement DSP algorithms. In this investigation, we developed an alternative approach based on an embedded FPGA system for image processing. Field Programmable Gate Array (FPGA) is widely used in embedded applications such as automotive, communications, industrial automation, motor control, medical imaging etc. FPGA is chosen due to its reconfigurable ability. Without requiring hardware change-out, the use of FPGA type devices expands the product life by updating data stream files. FPGAs have grown to have the capability to hold an entire system on a single chip meanwhile, it allows in-platform testing and debugging of the system. Furthermore, it offers the opportunity of utilizing hardware/software co-design to develop a high performance system for different applications by incorporating processors (hardware core processor or software core processor), on-chip busses, memory, and hardware accelerators for specific software functions.

In this paper, video surveillance a -based image processing system is developed on a Xilinx Spartan3 Field Programmable Gate Array (FPGA) device using an embedded development kit (EDK) from Xilinx. Video surveillance is one of the most popular transform coding techniques for image and video Segmentation. The video processing and image compression standards such as JPEG, MPEG, and H.26x have adopted as video surveillance the transform coder [1-3]. Consequently, video surveillance is chosen as the application algorithm for the embedded system. This paper is organized as follows: Section II briefly

reviews Back Ground Subtraction method. Section III discusses the design flow. Section IV covers different architecture for video surveillance co-processor and compares their performance. Section V is the conclusion part.

II. MOVING OBJECT DETECTION

A. Moving Object Extraction

After the background image B(x, y) is obtained, subtract the background image B(x,y) from the current frame Fk (x, y). If the pixel difference is greater than the set threshold T , then determines that the pixels appear in the moving object, otherwise, as the background pixels. The moving object can be detected after threshold operation. Its expression is as follows:

$$D_k(x,y)=\begin{cases}1 & |F_k(x,y)-B_{k-1}(x,y)|>T \\ 0 & \text{others}\end{cases} \quad .....(3)$$

Where Dk (x, y) is the binary image of differential results. T is gray-scale threshold, its size determines the accuracy of object identification. As in the algorithm T is a fixed value, only for an ideal situation, is not suitable for complex environment with lighting changes. Therefore, this paper proposes the dynamic threshold method, we dynamically changes the threshold value according to the lighting changes of the two images obtained.

B. Extraction of Moving Human Body

After median filtering and morphological operations, some accurate edge regions will be got, but the region belongs to the moving human body could not be determined. Through observation, we can find out that when moving object appears, shadow will appear in some regions of the scene. The presence of shadow will affect the accurate extraction of the moving object. By analyzing the characteristics of motion detection, we combine the projection operator with the previous methods. Based on the results of the methods above, adopting the method of combining vertical with horizontal projection to detect the height of the motion region. This can eliminate the impact of the shadow to a certain degree. Then we analyze the vertical projection value and set the threshold value (determined by experience) to remove the pseudo-local maximum value and the pseudo-local minimum value of the vertical projection to determine the number and width of the body in the motion region, we will get the moving human body with precise edge. This article assumes that people in the scene are all in upright-walking state.

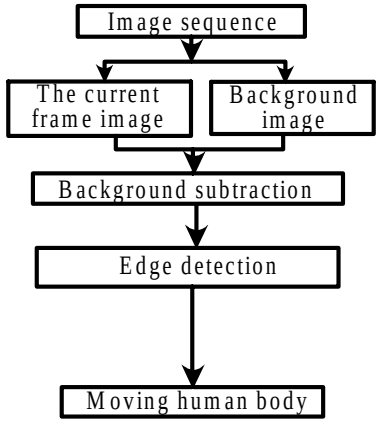

Figure 1: *The flow chart of moving human body extraction*

Human body detection is to identify the corresponding part of human from the moving region. But the extracted moving region may correspond to different moving objects, such as pedestrians, vehicles and other such birds, floating clouds, the swaying tree and other moving objects. Hence we use the shape features of motion regions to further determine whether the moving object is a human being. Judging criteria are as follows the object area is larger than the set threshold the aspect ratio of the object region should conform to the set ratio. If these two conditions are met, the moving object is the moving human body, or is not a human body.

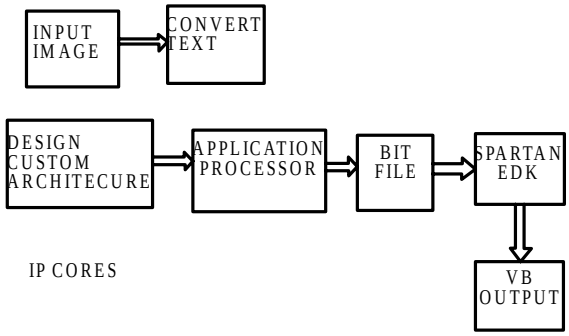

Fig2: *block diagram*

III. ARCHITECTURE

To build an embedded system on Xilinx FPGAs, the embedded development kit (EDK) is used to complete the reconfigurable design. Figure 1 shows the design flow.

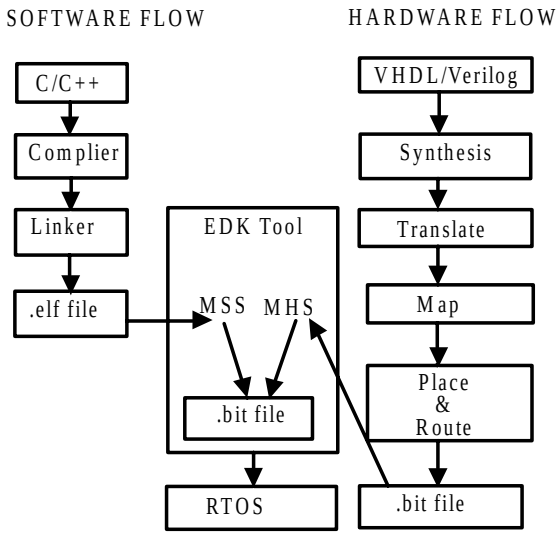

Fig 2 : *Design flow*

Unlike the design flow in the traditional software design using C/C++ language or hardware design using hardware description languages, the EDK enables the integration of both hardware and software components of an embedded system. For the hardware side, the design entry from VHDL/Verilog is first synthesized into a gate-level netlist, and then translated into the primitives, mapped on the specific device resources such as Look-up tables, flip-flops, and block memories. The location and interconnections of these device resources are then placed and routed to meet with the timing Constraints. A downloadable .bit file is created for the whole hardware platform. The software side follows the standard embedded software flow to compile the source codes into an executable and linkable file (ELF) format. Meanwhile, a microprocessor software specification (MSS) file and a microprocessor hardware specification (MHS) file are used to define software structure and hardware connection of the system. The EDK uses these files to control the design flow and eventually merge the system into a single downloadable file. The whole design runs on a real-time operating system (RTOS).

IV. VIDEO SURVILLANCE CO-PROCESSOR

There are different ways to include processors inside Xilinx FPGA for System-on-a-Chip (SoC): PowerPC hard processor core, or Xilinx MicroBlaze soft processor core, or user-defined soft processor core in VHDL/Verilog. In this work, The 32-bit MicroBlaze processor is chosen because of the flexibility. The user can tailor the processor with or without advance features, based on the budget of hardware. The advance features include memory management unit, floating processing unit, hardware multiplier, hardware divider, instruction and data cache links etc. The architecture overview of the system is shown in Figure 2. It can be seen that there are two different buses (i.e., processor local bus (PLB) and fast simplex link (FSLbus) used in the system [5-6]. PLB follows IBM core connect bus architecture, which supports high bandwidth master and slave devices, provides up to 128- bit data bus, up to 64-bit address bus and centralized bus Arbitration. It is a type of shared bus. Besides the access overhead, PLB potentially has the risk of hardware/software incoherent due to bus arbitration. On the other hand, FSL supports point-to-point unidirectional communication. A pair of FSL buses (from processor to peripheral and from peripheral to processor) can form a dedicated high speed bus without arbitration mechanism. Xilinx provides C and assembly language support for easy access. Therefore, most of peripherals are connected to the processor through PLB; the DWT coprocessor is connected through FSL instead.

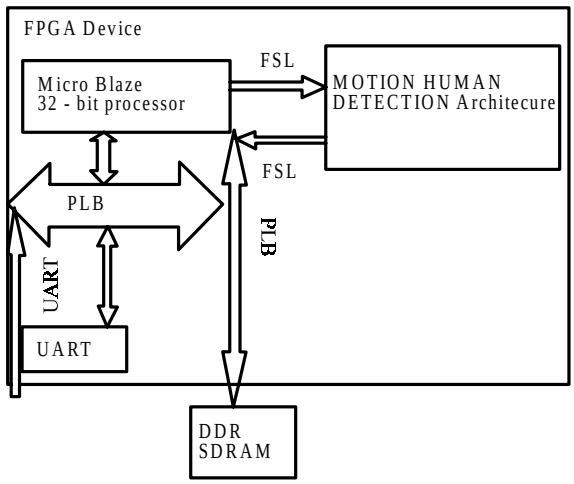

Fig 3 : *System Overview*

The current system offers several methods for distributing the data. These methods are a UART, and VGA, and Ethernet controllers. The UART is used for providing an interface to a host computer, allowing user interaction with the system and facilitating data transfer. The VGA core produces a standalone real-time display. The Ethernet connection allows a convenient way to export the data for use and analysis on other systems. In our work, to validate the DWT coprocessor, an image data stream is formed using VISUAL BASIC, then transmitted from the host computer to FPGA board through UART port.

V.EXPERIMENTAL RESULTS

Experiments are performed on gray level images to verify the proposed method. These images are represented by 8 bits/pixel and size is 128 x 128. Image used for experiments are shown in below figure.

Figure 4 : *background images*

The measurands used for proposed method are as follows:

The entropy (E) is defined as Where s is the set of processed coefficients and p (e) is the probability of processed coefficients. By using entropy, number of bits required for compressed image is calculated. An often used global objective quality measure is the mean square error (MSE) defined as Where, nxm is the number of total pixels. f (i,j) and f(i,j)' are the pixel values in the original and reconstructed image. The peak to peak signal to noise ratio (PSNR in dB) [11-13] is calculated as

Figure 5 : *current image*

Figure 6 : *output image*

And the synthesis report is below

```
Selected Device : 3s500efg320-4

 Number of Slices:                  2649  out of   4656    56%
 Number of Slice Flip Flops:        3343  out of   9312    35%
 Number of 4 input LUTs:            3794  out of   9312    40%
    Number used as logic:           3118
    Number used as Shift registers:  356
    Number used as RAMs:             320
 Number of IOs:                       83
 Number of bonded IOBs:               40  out of    232    17%
    IOB Flip Flops:                   55
 Number of BRAMs:                      7  out of     20    35%
 Number of MULT18X18SIOs:              3  out of     20    15%
 Number of GCLKs:                      7  out of     24    29%
 Number of DCMs:                       2  out of      4    50%

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 12.384ns (Maximum Frequency: 80.749MHz)
   Minimum input arrival time before clock: 41.553ns
   Maximum output required time after clock: 13.840ns
   Maximum combinational path delay: 3.344ns
```

Fig. 7 : *Synthesis report*

VI. CONCLUSIONS

In this paper, a Background Subtraction-based reconfigurable system is designed using the EDK tool. Hardware architectures of Motion human detection algorithm have been implemented as a coprocessor in an embedded system. the hardware cost of these architecture is compared for benchmark images. This type of work using EDK can be extended to other applications of embedded system. These two architectures applications compared for benchmark images. This type of work using EDK can be extended to other applications of embedded systems.

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Implement Discrete Wavelet Transform and Principal Component Analysis to Digital Video Watermarking

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ABSTRACT

Digital Watermarking is a technology used for the copyright protection of digi applications. In this paper, a comprehensive approach for watermarking digit video is introduced. We propose a hybrid digital video watermarking scheme based on Discrete Wavelet Transform (DWT) and Principal Component Analysis (PCA). PCA helps in reducing correlation among the wavelet coefficients obtained from wavelet decomposition of each video frame thereby dispersing the watermark bits into the uncorrelated coefficients. The video frames are first decomposed using DWT and the binary watermark is embedded in the principal components of the low frequency wavelet coefficients. The imperceptible high bit rate watermark embedded is robust against various attacks that can be carried out on the watermarked video, such as filtering, contrast adjustment, noise addition and geometric attacks.

Keywords

Digital video; binary watermark; Discrete Wavelet Transform; Principal Component Analysis.

I. INTRODUCTION

The popularity of digital video based applications [1] is accompanied by the need for copyright protection to prevent illicit copying and distribution of digital video. Copyright protection inserts authentication data such as ownership information and logo in the digital media without affecting its perceptual quality. In case of any dispute, authentication data is extracted from the media and can be used as an authoritative proof to prove the ownership. As a method of copyright protection, digital video watermarking [2, 3] has recently emerged as a significant field of interest and a very active area of research.

Watermarking is the process that embeds data called a watermark or digital signature into a multimedia object such that watermark can be detected or extracted later to make an assertion about the object. The object may be an image or audio or video. For the purpose of copyright protection digital watermarking techniques must meet the criteria of imperceptibility as well as robustness against all attacks [4-6] for removal of the watermark.

Many digital watermarking schemes have been proposed for still images and videos [7]. Most of them operate on uncompressed videos [8-10], while others embed watermarks directly into compressed videos [8,11]. The work on video specific watermarking can be further found in [12-15]. Video watermarking introduces a number of issues not present in image watermarking. Due to inherent redundancy between video frames, video signals are highly susceptible to attacks such as frame averaging, frame dropping, frame swapping and statistical analysis.

Video watermarking approaches can be classified into two main categories based on the method of hiding watermark bits in the host video. The two categories are: Spatial domain watermarking where embedding and detection of watermark are performed by directly manipulating the pixel intensity values of the video frame. Transform domain [16-18] techniques, on the other hand, alter spatial pixel values of the host video according to a pre-determined transform and are more robust than spatial domain techniques since they disperse the watermark in the spatial domain of the video frame making it difficult to

remove the watermark through malicious attacks like cropping, scaling, rotations and geometrical attacks.

The commonly used transform domain techniques are Discrete Fourier Transform (DFT), the Discrete Cosine Transform (DCT), and the Discrete Wavelet Transform (DWT). In this paper, we propose an imperceptible and robust video watermarking algorithm based on Discrete Wavelet Transform (DWT) [19-25] and Principal Component Analysis (PCA) [26-28]. DWT is more computationally efficient than other transform methods like DFT and DCT. Due to its excellent spatio-frequency localization properties, the DWT is very suitable to identify areas in the host video frame where a watermark can be embedded imperceptibly. It is known that even after the decomposition of the video frame using the wavelet transformation there exist some amount of correlation between the wavelet coefficients. PCA is basically used to hybridize the algorithm as it has the inherent property of removing the correlation amongst the data i.e. the wavelet coefficients and it helps in distributing the watermark bits over the sub-band used for embedding thus resulting in a more robust watermarking scheme that is resistant to almost all possible attacks. The watermark is embedded into the luminance component of the extracted frames as it is less sensitive to the human visual system (HVS).

The paper is organized as follows. Section II contains the watermarking scheme. Section III contains the experimental results and finally Section IV gives the conclusion.

II. WATERMARKING SCHEME

The watermarking algorithm basically utilizes two mathematical techniques: DWT and PCA. The significance of using these techniques in watermarking has been explained first.

A. Discrete Wavelet Transform:

The Discrete Wavelet Transform (DWT) is used in a wide variety of signal processing applications.

2-D discrete wavelet transform (DWT) decomposes an image or a video frame into sub-images, 3 details and 1 approximation. The approximation sub-image resembles the original on 1/4 the scale of the original. The 2-D DWT (Figure. 1) is an application of the 1-D DWT in both the horizontal and the vertical directions. DWT separates the frequency band of an image into a lower resolution approximation sub-band (LL) as well as horizontal (HL),vertical (LH) and diagonal (HH) detail components.

Embedding the watermark in low frequencies obtained by wavelet decomposition increases the robustness with respect to attacks that have low pass characteristics like filtering, lossy compression and geometric distortions while making the scheme more sensitive to contrast adjustment, gamma correction, and histogram equalization. Since the HVS is less sensitive to high frequencies, embedding the watermark in high frequency sub-bands makes the watermark more imperceptible while embedding in low frequencies makes it more robust against a variety of attacks.

LL_1	HL_1
LH_1	HH_1

Figure 1:*DWT subbands*

B. Principal Component Analysis

Principal component analysis (PCA) is a mathematical procedure that uses an orthogonal transformation to convert a set of observations of possibly correlated variables into a set of values of uncorrelated variables called principal components. The number of principal components is less than or equal to the number of original variables. PCA is a method of identifying patterns in data, and expressing the data in such a way so as to highlight their similarities and differences. Since patterns in data can be hard to find in data of high dimension, where the advantage of graphical representation is not available, PCA is a powerful tool for analyzing data. The other main advantage of PCA is that once these patterns in the data have been identified, the data can be compressed by reducing the number of dimensions, without much loss of information. It plots the data into a new coordinate system where the data with maximum covariance are plotted together and is known as the first principal component. Similarly, there are the second and third principal components and so on. The maximum energy concentration lies in the first principal component.

The following block diagram (Figure.2) shows the embedding and extraction procedure of the watermark. In the proposed method the binary watermark is embedded into each of the video frames by the decomposition of the frames into DWT sub bands followed by the application of block based PCA on the sub-blocks of the low frequency sub-band. The watermark is embedded into the principal components of the sub-blocks. The extracted watermark is obtained through a similar procedure.

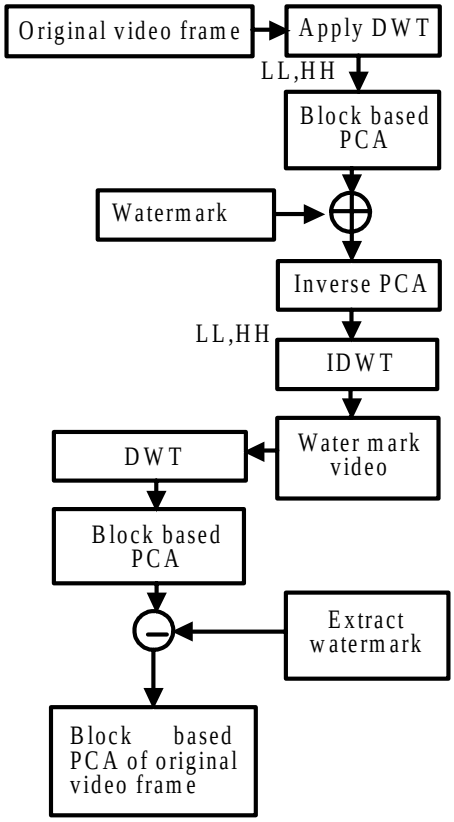

Figure2: *Block Diagram of Watermarking*

C. Algorithms for watermarking using DWT AND PCA

Algorithm 1:

a) Embedding Procedure

Step 1: Convert the $n \times n$ binary watermark logo into a vector $W = \{w_1, w_2 ..... , w_{n \times n}\}$ of '0's and '1's.

Step 2: Divide the video $(2N \times 2N)$ into distinct frames.

Step 3: Convert each frame from RGB to YUV colour format.

Step 4: Apply 1-level DWT to the luminance (Y component) of each video frame to obtain four sub-bands LL, LH , HL and HH of size $N \times N$.

Step 5: Divide the LL sub-band into k non-overlapping sub-blocks each of dimension $n \times n$ (of the same size as the watermark logo).

Step 6: The watermark bits are embedded with strength α into each sub-block by first obtaining the principal component scores by Algorithm 2. The embedding is carried out as equation 1.

$$Score_i^{'} = score_i + \alpha W \qquad .....(1)$$

where $score_i$ represents the principal component matrix of the i^{th} sub-block.

Step 7 : Apply inverse PCA on the modified PCA Components of the sub-blocks of the LL sub-band to obtain the modified wavelet coefficients.

Step 8: Apply inverse DWT to obtain the watermarked luminance component of the frame. Then convert the video frame back to its RGB components.

b) Extraction Procedure

Step 1: Divide the watermarked (and possibly attacked) video into distinct frames and convert them from RGB to YUV format.

Step 2: Choose the luminance (Y) component of a frame and apply the DWT to decompose the Y component into the four sub-bands LL , HL , LH , and HH of size $N \times N$.

Step 3: Divide the LL sub-band into $n \times n$ non overlapping sub-blocks.

Step 4: Apply PCA to each block in the chosen subband LL by using Algorithm 2.

Step 5: From the LL sub-band, the watermark bits are extracted from the principal components of each sub-block as in equation 2.

$$W_i^{'} = \frac{\left(score_i^{'} - score_i\right)}{\alpha} \qquad .....(2)$$

where $W_i^{'}$ is the watermark extracted from the i^{th} sub block.

Algorithm 2:

The LL sub-band coefficients are transformed into a new coordinate set by calculating the principal components of each sub-block $(\text{size}\, n \times n)$.

Step 1: Each sub-block is converted into a row vector D_i with n_2 elements (i = 1,2…k).

Step 2: Compute the mean μ_i and standard deviation σ_i of the elements of vector D_i .

Step 3: Compute Z_i according to the following equation

$$Z_i = \frac{D_i - \mu_i}{\sigma_i} \qquad .....(3)$$

Here Z_i represents a centered, scaled version of D_i , of the same size as that of D_i .

Step 4: Carry out principal component analysis on $i\ Z$ $(\text{size}1\times n_2)$ to obtain the principal component coefficient matrix coeffi $(\text{size}\,n2\times n2)$.

Step 5: Calculate vector score_i as

$$\text{score}_i = Z_i * \text{coeffi}_i \qquad \text{.....(4)}$$

where score_i represents the principal component scores of the i^{th} sub-block.

III. EXPERIMENTAL RESULTS

The proposed algorithm is applied to a sample video sequence 'SUZIE.AVI' using a 32×32 watermark logo. The grayscale watermark is converted to binary before embedding. Figure. 3(a) and 3(b) show the original and the watermarked video frames respectively. Figure. 4(a) is the embedded watermark and Figure. 4(b) is the extracted binary watermark image.

The performance of the algorithm has been measured in terms of its imperceptibility and robustness against the possible attacks like noise addition, filtering, geometric attacks etc.

Figure 3(a): *Original video frame*

(a) *(b)*

Figure 4 : *(a) Original watermark (b) Extracted binary watermark*

Figure 3(b) : *watermarked video*

PSNR **:** The Peak-Signal-To-Noise Ratio (PSNR) is used to deviation of the watermarked and attacked frames from the original video frames and is defined as:

$$\text{PSNR} = 10\log_{10}\left(225^2/\text{MSE}\right) \qquad \text{.....(5)}$$

where MSE (mean squared error) between the original and distorted frames $(\text{size}\,m\times n)$ is defined as:

$$\text{MSE} = (1/mn)\sum_{i=1}^{m}\sum_{j=1}^{n}[i,j]-I'(i,j) \qquad \text{.....(6)}$$

where *I* and *I*? are the pixel values at location (i, j) of the original and the distorted frame respectively. Higher values of PSNR indicate more imperceptibility of watermarking. It is expressed in decibels (dB).

NC **:** The normalized coefficient (NC) gives a measure of the robustness of watermarking and its peak value is 1.

$$\text{NC} = \frac{\sum_{i=1}^{m}\sum_{j=1}^{n} W(i,j), W'(i,j)}{\sqrt{\sum_i\sum_j (i,j)}\sqrt{\sum_i\sum_j W'(i,j)}} \qquad \text{.....(7)}$$

Where *W* and *W*? represent the original and extracted watermark respectively. After extracting and refining the watermark, a similarity measurement of the extracted and the referenced watermarks is used for objective judgment of the extraction fidelity. The following images represent stills taken from the watermarked video in after tacks have been carried on it.

Figure 5 : *video frame after addition of Gaussian noise*

Figure 6: *video frame after addition of 'salt and pepper' noise*

Figure 7: *video frame after rotation by 5 degrees*

Figure 8: *video frame after resizing*

Figure 9: *video frame after cropping*

Figure 10: *video frame after Gamma correction*

Figure 11: *video frame after addition of poission noise*

Figure 12: *video frame after applying Contrast Adjustment*

Figure 13: *video frame after Median filtering*

ATTACK	PSNR	NC
GAUSSIAN NOISE	54.27	0.0030
SALT & PEPPER NOISE	40.61	0.0031
CROPPING	20.97	0.0019
ROTATION	27.45	0.0026
RESIZING	57.62	0.0031
MEDIAN FILTERING	82.40	0.0030
GAMMA CORRECTION	32.46	0.0024
CONTRAST ADJUSTMENT	48.24	0.0029
Poission noise	55.97	0.0030

Table I: *Result Analysis*

Figure. 5 and Figure. 6 show the watermarked video frame after the addition of gaussian noise and 'salt and pepper' noise respectively. Figure. 7 shows the effect of carrying out video frame rotation by an angle of 5 degrees. Figure. 8 shows the watermarked video frame after resizing first by a factor of half followed by a factor to 2 to return it to its original size. Figure. 9 shows the cropped video frame. Figures 10-12 show the effect of applying gamma correction (variance0.5), poission noise and contrast adjustment. Figure. 13 show the resultant video median filter (3×3 box filter) respectively.

The following table shows the value of the data collected from the watermarked video after performing the various attacks as shown previously.

IV CONCLUSION AND FUTURE WORK

The algorithm implemented using DWT-PCA is robust and imperceptible in nature and observing the PSNR, MSE and NC by applying different attacks to the video frames and the video frames can be subject to scene change analysis to embed an independent watermark in the sequence of frames forming a scene, and repeating this procedure for all the scenes within a video.

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Poisson Image Denoising Using Modified Anscombe Transformation

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ABSTRACT

Removal of Poisson noise from images is a difficult task because, Poisson noi is signal dependent, as compared to other kind of noises. The commonly us approach for the removal of Poisson noise is an indirect way consisting of three steps. First, stabilization of noise variance using Anscombe root transformation producing a signal in which the noise can be treated as additive Gaussian with unitary variance. Second, the noise is removed using a conventional de noising algorithm for additive white Gaussian noise. Third, an inverse transformation is applied to the denoised signal, obtaining the estimate of the original image. As the forward transformation using here is nonlinear choice of direct inverse transformations results in bias and errors in estimation. Existing two methods of inverse transformations are direct algebraic inverse and asymptotically unbiased inverse proposed by Anscombe. Asymptotically unbiased inverse provides unbiasedness only asymptotically for large intensities, while at low counts it leads to a larger bias than the direct algebraic inverse. Here 3 optimal inverse transformations for Anscombe root transformation is proposed, exact unbiased inverse, a maximum likelihood (ML) inverse and minimum mean square error (MMSE) inverse.

Keywords

Denoising, Poisson noise, Variance stabilization.

I. INTRODUCTION

Removal of Poisson noise from images is important for many applications as it is a characteristic of many image acquisition systems especially in astronomy and medical imaging. In case of poisson noise, variance and the expected value of the noise affecting the pixel is the same, ie; poisson noise is signal dependent. So denoising of poisson noise affected image is different and difficult as compared to the case of additive white Gaussian noise with constant variance typically assumed by signal processing filters for noise removal.

The removal of poisson noise is performed through the following three-step procedure. First, the noise variance is stabilized by applying the Anscombe root transformation to the data. This produces a signal in which the noise can be treated as additive Gaussian with unitary variance. Second, the noise is removed using a conventional denoising algorithm for additive white Gaussian noise. Third, an inverse transformation is applied to the denoised signal, obtaining the estimate of the signal of interest. The Anscombe transformation is done using the function f given by,

$$f : z \rightarrow 2\sqrt{z + 3/8} \qquad \text{.....(1)}$$

The choice of the proper inverse transformation is crucial in order to minimize the bias error which arises when the nonlinear forward transformation is applied. Both the algebraic inverse and the asymptotically unbiased inverse proposed by Anscombe lead to a significant bias at low counts. In particular, the latter inverse provides unbiasedness only asymptotically for large counts while at low counts it leads to a larger bias than the former one.

Here first an exact unbiased inverse is proposed and later its shown to be coinciding with a maximum likelihood inverse and then a minimum mean square error inverse (MMSE) is also proposed. In particular, the combination of BM3D and the exact unbiased inverse outperforms some of the best existing algorithms specifically targeted at Poisson noise removal, while maintaining low computational complexity. BM3D is one of the best existing methods for denoising of images affected by Gaussian

noise. Here i had done the Gaussian noise removal by wiener filter which is also performs good in removal of Gaussian noise.

II. PRELIMINARIES

A. Poisson Noise

Let z_i , i = 1,2,...,N be the observed pixel values obtained through an image acquisition device. It can interpret the image affected by poisson noise as, each z_i to be an independent random Poisson variable whose mean $y_i \geq 0$ is the underlying intensity value to be estimated. The discrete Poisson probability of each z_i is,

$$P(z_i / y_i) = \frac{y_i^{zi} e^{-yi}}{z_i!} \quad .....(1)$$

Here the parameter y_i is the mean and variance of poisson variable z_i .

$$E\{z_i / y_i\} = y_i = \text{var}\{z_i / y_i\} \quad (2)$$

Poisson noise can be modelled as,

$$n_i = z_i - E\{z_i / y_i\} \quad (3)$$

So that $E\{n_i / y_i\} = 0$ and $\text{var}\{n_i / y_i\} = y_i$

Since the noise variance depends upon the true intensity value, Poisson noise is signal dependent. More specifically,

The standard deviation of the noise n_i equals y_i . Due to this, the effect of Poisson noise increases (i.e., the signal-to noise ratio decreases) as the intensity value decreases.

B. Variance Stabilization and the Anscombe Transformation

Variance-stabilizing transformation is applying to remove the data-dependence of the noise variance, so that it becomes constant throughout the whole data. Moreover, if the transformation is also normalizing (i.e; it results in a Gaussian noise distribution), we can estimate the intensity values with a conventional denoising method designed for additive white Gaussian noise. But neither exact stabilization nor exact normalization are possible and therefore, in practice, approximate or asymptotical results are employed.

One of the most popular variance-stabilizing transformations is the Anscombe transformation,

$$f : z \rightarrow 2\sqrt{z + 3/8} \quad .....(4)$$

By applying this transformation in Poisson distributed data gives a signal whose noise is asymptotically additive standard normal. The denoising of f(z) produces a signal D that can be considered as an estimate of E{*f*(*z*)/*y*}. We need to apply an inverse transformation to D in order to obtain the desired estimate of y. The direct algebraic inverse of (4) is,

$$I_A(D) = f^{-1}(D) = (D/2)^2 - 3/8 \quad .....(5)$$

But the resulting estimate of is biased. Because for a nonlinear transformation f,

$$E\{f(z/y)\} \neq f(E\{z/y\}) \quad .....(6)$$

and hence

$$f^{-1}(E\{f(z/y)\}) \neq E\{z/y\} \quad .....(7)$$

Another existing inverse is,

$$I_B(D) = (D/2)^2 - 1/8 \quad .....(8)$$

which provides asymptotically unbiasedness for large counts (intensity)

III. OPTIMAL INVERSE TRANSFORMATIONS

While the asymptotically unbiased inverse (8) provides good results for high-count data, applying it to low-count data leads to a biased estimate and direct inverse provides bias more for high counts. Here 3 types of optimal inverses are proposed.

A. Exact Unbiased Inverse

An optimal inverse is an inverse transformation I_C which maps the values $E\{f(z/y)\}$ to the desired value $E\{z/y\}$ As $E\{z/y\}$ = y finding the inverse I_C reduces to computing the values $E\{f(z/y)\}$ and then do an inverse mapping to get y corresponds to each $E\{f(z/y)\}$.

$$E\left\{f\left(\frac{z}{y}\right)\right\} = \int_{-\infty}^{\infty} f(z) P\left(\frac{z}{y}\right) dz \quad .....(9)$$

In case of image, Poisson probability P(z/y) is discrete and image will be having only positive values, so we can modify the equation(9) as,

$$E\left\{f\left(\frac{z}{y}\right)\right\} = \sum_{-\infty}^{\infty} f(z) P\left(\frac{z}{y}\right) \quad .....(10)$$

$$= 2\sum_{-\infty}^{\infty} \sqrt{z + \frac{3}{8}} . \frac{d^{-y} y^z}{z!} \quad .....(11)$$

Figure. 1 shows the plots of the inverse transformations I_A, I_B and I_C . Since I_C is unbiased, it's clear from the figure that at low counts the asymptotically unbiased inverse actually leads to a larger bias than the algebraic inverse. If the denoised data D is having some errors, ie; $D \neq E\{f(z/y)\}$, then the estimation error in

$y = I_C(D)$ can include variance as well as bias components. So the unbiasedness of I_C holds only if $D = E\{f(z/y)\}$.

Figure.1.Inverse Anscombe transformations I_A *(algebraic),* I_B *(asymptotically unbiased) and* I_C *(exact unbiased).*

For simplicity in implementation the exact unbiased inverse can be expressed in a approximated closed form [2] given by,

$$\bar{I}_C(D) = \frac{1}{4}D^2 + \frac{1}{4}\sqrt{\frac{3}{2}}D^{-1} - \frac{11}{8}D^{-2} + \frac{5}{8}\sqrt{\frac{3}{2}}D^{-3} - \frac{1}{8} \quad (12)$$

B. ML Inverse

ML inverse is based on a more general scenario where we will consider that $D \neq E\{f(z/y)\}$ and we assume that the point wise MSE of D as an estimate of $E\{f(z/y)\}$ is

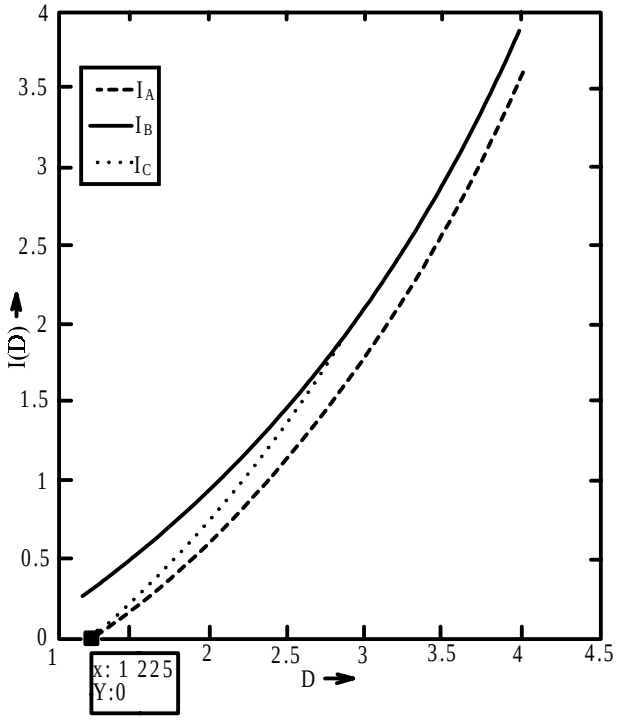
$$\varepsilon^2 = E\{(D - E\{f(z/y)\})^2\} \quad .....(13)$$

The actual distribution of D is unknown. For simplicity, assume that D is normally distributed around $E\{f(z/y)\}$ with variance ε^2

$$D = N(E\{f(z/y)\}, a^{o2}) \quad .....(14)$$

so that D can be considered as an unbiased estimate of $E\{f(z/y)\}$. We can find out the ML estimate of D as,

$$D_{ML} = \text{ary}\max_y(p(D/y)) \quad .....(15)$$



where,

$$P(D/y) = \frac{1}{\sqrt{2\Pi\varepsilon^2}} e^{-\frac{1}{2\varepsilon^2}(D - E\{f(z/y)\})^2} \quad .....(16)$$

By finding log likelihood function and differentiating with respect to D and equate to 0 we will get the ML estimate of D as,

$$D_{bML} = E\{f(z/y)\} \quad .....(17)$$

so that both ML inverse estimate and exact unbiased estimate coincides. Thus ML inverse is given by,

$$I_{ML}(D) = \begin{cases} I_C(D) & \text{if } D \geq 2\sqrt{3/8} \\ 0 & \text{if } D < 2\sqrt{3/8} \end{cases}$$

Here $I_{ML}(D)$ is independent of ε, and this result holds whenever D-E{*f*(*z*/*y*)} has a fixed unimodal distribution with mode at 0.

C. MMSE Inverse

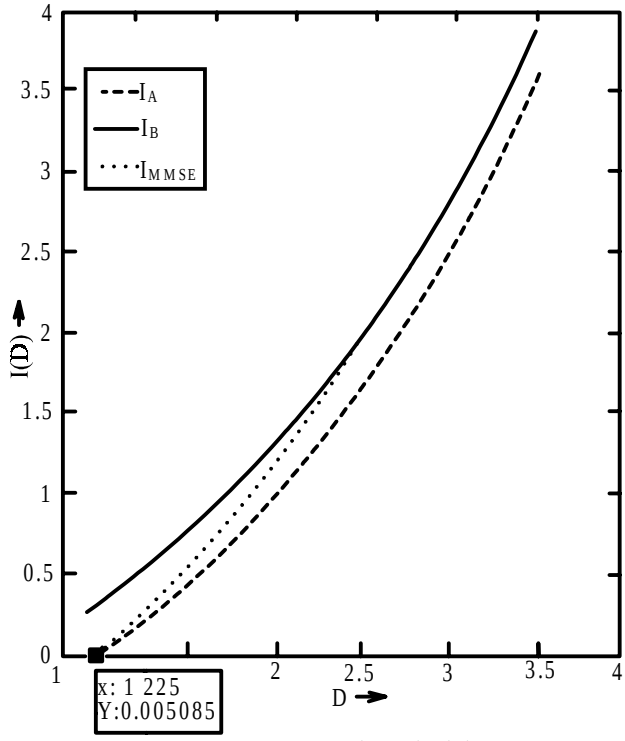
Under the same assumption as for ML estimation, MMSE inverse parameterised by ε is defined as,

$$I_{MMSE}(D,\varepsilon) = \arg\min_y\left(E\{(y-y)^2/D\}\right)$$

$$\Rightarrow \quad I_{MMSE}(D,\varepsilon) = \arg\min_y \int_{-\infty}^{+\infty} p(y/D)(y-y)^2 dy$$

According to Bayes's theorem,

$$p(y/D) = \frac{P(D/y)p(y)}{p(D)} \quad .....(20)$$



$$\Rightarrow I_{MMSE}(D,\varepsilon) = \arg\min_y \int_{-\infty}^{+\infty} \frac{P(D/y)p(y)}{p(D)}(y-y)^2 dy$$

$$\Rightarrow \quad I_{MMSE}(D,\varepsilon) = \arg\min_y \int_{-\infty}^{+\infty} P(D/y)p(y)(y-y)^2 dy$$

Assuming y to be uniformly distributed over R^+ region the equation can be reduces to,

$$I_{MMSE}(D,\varepsilon) = \arg\min_y \int_0^{\infty} P(D/y)(y-y)^2 dy \qquad .....(23)$$

By differentiating (23) and equating to 0 we will get the MMSE estimate of y as,

$$y = \frac{\int_0^{+\infty} P(D/y)ydy}{\int_0^{+\infty} P(D/y)dy} \qquad .....(24)$$

The exact unbiased inverse can be considered a limit case of the MMSE inverse, obtained when $\varepsilon = 0$, ie;

$$I_{MMSE}(D,0) = I_C(D) = I_{ML}(D) \qquad .....(25)$$

Figure.2.Inverse Anscombe transformations I_A (algebraic), I_B (asymptotically unbiased) and I_{MMSE} (Minimum Mean Square Error).

Figure 3. MMSE inverse transformations for some values of ε.

IV. EXPERIMENTS

The test images used in experiments are shown in figure 4. All experiments done consist of the same three-step denoising procedure: First we apply the forward Anscombe transformation (4) to a noisy image. Then we denoise the transformed image (Assuming additive white Gaussian noise with unit variance) with a Wiener filter, and finally we apply an inverse transformation in order to get the final estimate. As the inverse transformations for 3 methods are same for $\varepsilon = 0$ which is the general case anyone equation can be used for implementation. I used the MMSE integral equation with ε close to zero for inverse transformation.

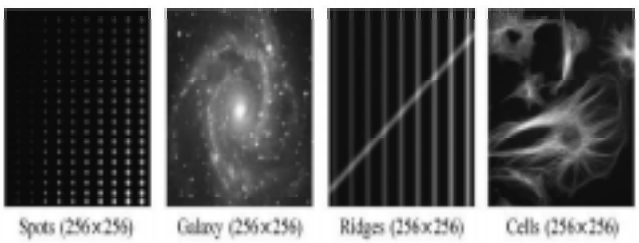


Figure. 4 : *Four test images used in experiments*

The results after image denoising for optimal inverse and asymptotically unbiased are shown in figure.5

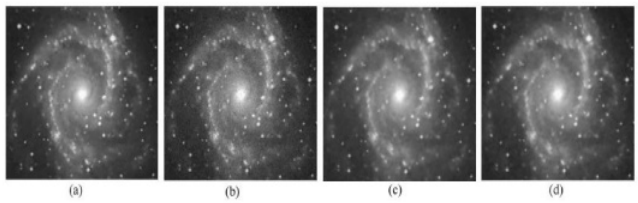


Figure.5.(a)Galaxy original image (b)Poisson-count image(c)Image denoised with wiener filter and asymptotically unbiased inverse (d)Image denoised with wiener filter and exact unbiased image

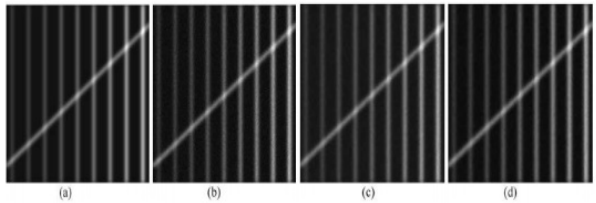
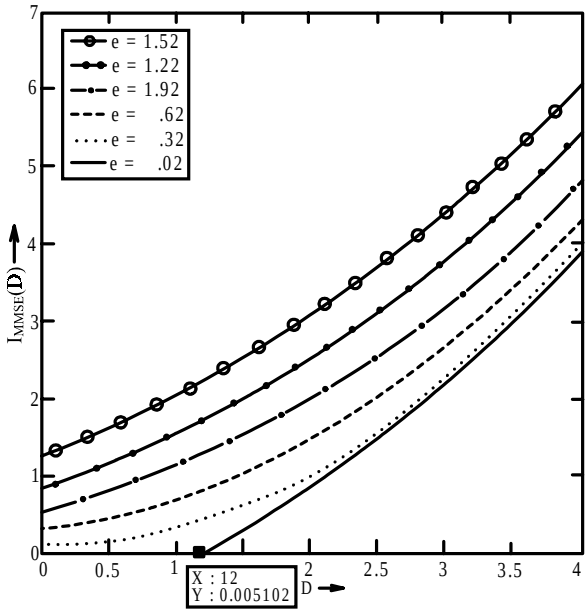


Figure.6 : *(a)Ridges original image (b)Poisson-count*



image(c)Image denoised with wiener filter and asymptotically unbiased inverse (d)Image denoised with wiener filter and exact unbiased image

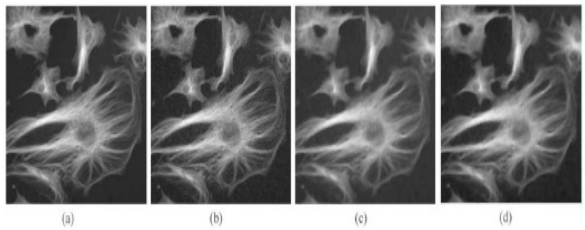


Figure.7.(a)Cells original image (b)Poisson-count image(c)Image denoised with wiener filter and asymptotically unbiased inverse (d)Image denoised with wiener filter and exact unbiased image

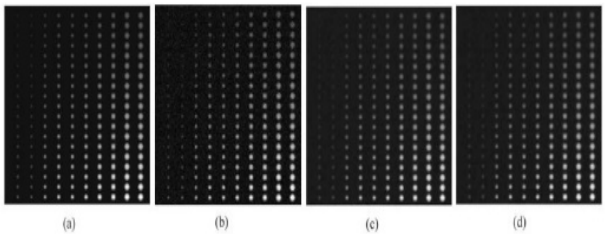


Figure.8.(a)Spots original image (b)Poisson-count image(c)Image denoised with wiener filter and asymptotically unbiased inverse (d)Image denoised with wiener filter and exact unbiased image

The performance of methods using asymptotically unbiased inverse and exact unbiased inverse is calculated using Normalized Mean Integrated square Error (NMISE) or by

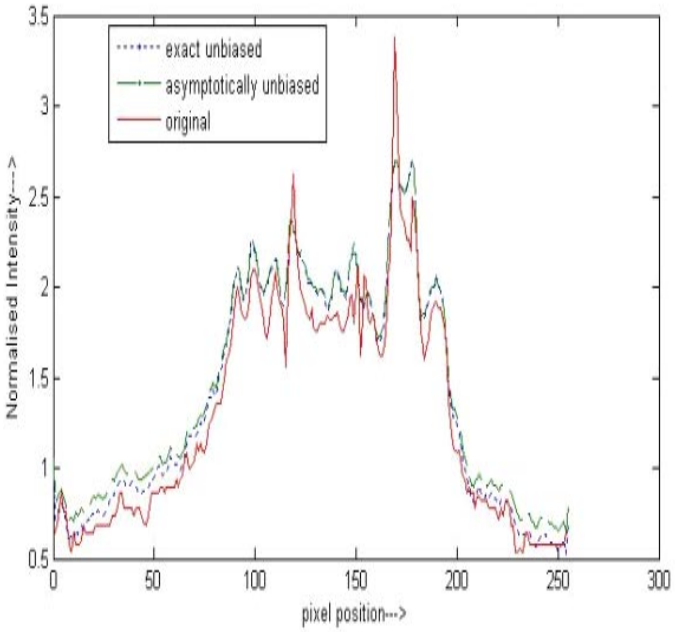
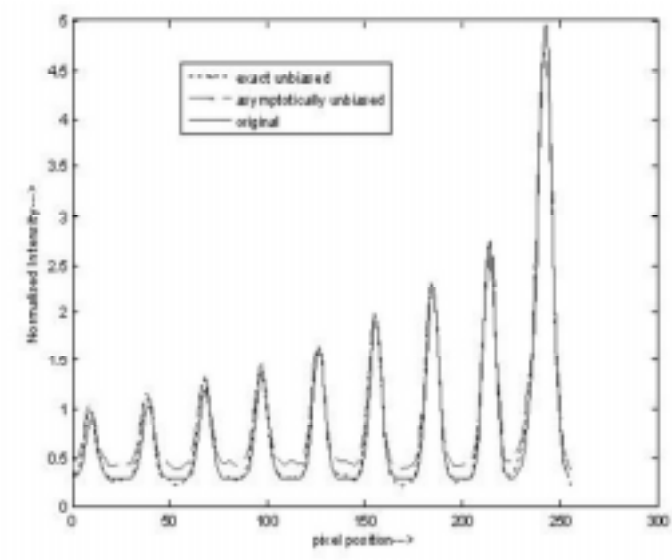


Fig. 9 : *Cross sections of original and denoised Cells image*



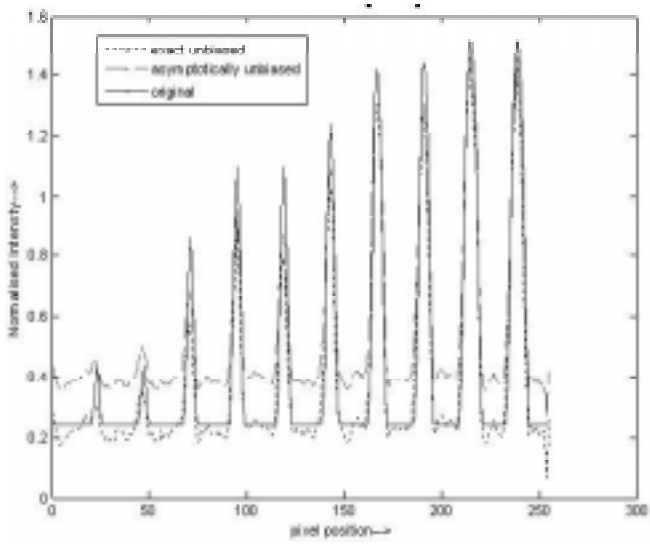


Figure.10 : *Cross section of original and denoised Ridges image*

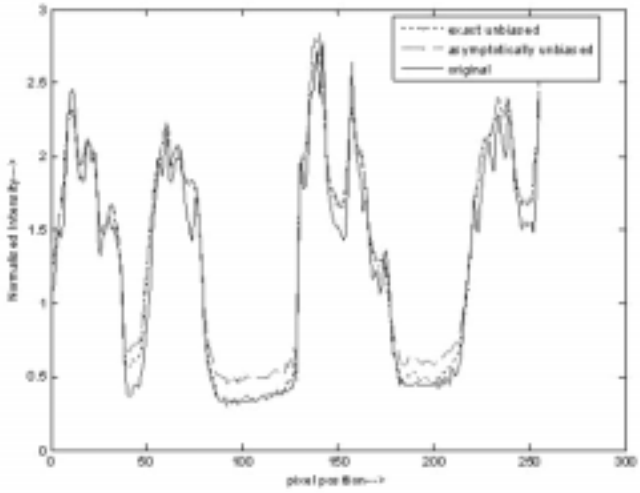


Figure.11 : *Cross section of original and denoised spot images*

Peak Signal to Noise Ratio(PSNR). The NMISE is calculated using the formula

$$\text{NMISE} = \frac{1}{\bar{N}} \sum_{i:y_i>0} \left((y_i - y_i)^2 / y_i \right)$$

$$\text{PSNR} = 10 \log_{10} \frac{\max_i (y_i)^2}{\sum_i \left((y_i - y_i)^2 / N \right)} \qquad \text{.....(26)}$$

where y_i are the estimated intensities, y_i the respective true values, and the sum is computed over the $\bar{N}$ pixels in the image for which $y_i > 0$.

The PSNR is calculated using the formula (26)

Obtained NMISE and PSNR values are shown in the figure 13

	Asymptocally unbiased inverse		Exact unbiased inverse	
	NMISE	PSNR	NMISE	PSMR
Galaxy	0.0587	25.7207	0.0144	30.9288
Ridges	0.1439	26.0012	0.0111	34.3125
Cells	0.1152	25.56710	.0170	31.4468
Spots	0.2485	25.92520	.0115	36.2640

Figure.13. NMISE and PSNR values of denoised images using asymptotically unbiased inverse and exact unbiased inverse.

V. CONCLUSION

In the recent years, variance stabilization has often been questioned as a viable method for Poisson noise removed because of the poor numerical results achieved at the low-count regime,i.e, for low intensity signals, which corresponds to the case of low signal to noise ratio(SNR). But the optimal inverse proposed here along with denoising methods such as BM3D will produce very good results in Poisson denoising images. Here i had done these experiments with simple wiener filter which is not so good as the best denoising methods for Gaussian noise removal such as BM3D, SAFIR, BLS-GSM, So the results are also not so good. But the effect when we are applying optimal inverse instead of asymptotically unbiased inverse is clearly understandable from the results.

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Analysis of Efficient Wavelet Based Image Compression Methods on Enhanced Medical Imagery

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ABSTRACT

For enhancing an image various enhancement schemes are used which includ gray scale manipulation, filtering and Histogram Equalization, Where Histogra equalization is one of the well known image enhancement technique. It became popular technique for contrast enhancement because it is simple and effecti The basic idea of Histogram Equalization method is to remap the gray levels of an image.

we analyze the influence of gamma correction of digital colour cameras on computer vision algorithms. The nonlinear signals R0, G0, and B0 yield a nonlinear shift in colour space models and can cause algorithms to fail. Use linear light signals R, G, and B for calculating most colour space models instead of the nonlinear signals R0, G0, and B0. In order to obtain linear light signals either the camera has to be configured linear using the gamma switch (if available) or by removing the nonlinearity analytically using the inverse operation (gamma re-correction).

Images require substantial storage and transmission resources, thus image compression is advantageous to reduce these requirements. signal and image processing are getting great improvements in performance by using wavelet based compression methods.

Comparative analysis of different enhancement and compression techniques will be carried out. This comparison will be done on the basis of subjective and objective parameters. Subjective parameters is visual quality and objective parameters are Peak signal-to- noise ratio (PSNR) , Compression Ratio(CR) ,Mean squared error (MSE) , L2-norm ratio , Bits per pixel(BPP) , Max. error.

Keywords

Histogram Equalization, gamma correction, wavelet, Medical image compressi

I. INTRODUCTION

Medical image enhancement technologies have become popular since advanced medical equipments were used in the medical field .Enhanced images are desired by a surgeon to assist diagnosis and interpretation because medical image qualities are often deteriorated by noise during acquiring and illumination condition. Image quality enhancement algorithms are developed to improve the visual appearance of an image by the increment of contrast, adjustment of brightness, and enhancing visually important features .Image enhancement is very important pre-processing stage in most image processing applications.

The nonlinear effects aren't consistent across all regions of the image. In other words, the value of gamma may change from one region to another . For example, it is possible that a scene contains a large dynamic illumination range that an imaging device is not able to adequately capture. Thus, especially in very dark or bright regions of the image, some details may become clustered together within a small intensity range . Hence a local enhancement process adjusts the image quality in different regions in such a way that the human viewers grasp these details.

There are two categories of Image enhancement methods : spatial domain methods and frequency domain methods. The spatial domain methods operate on image

pixels directly, such as: histogram equalization[1], gamma correction[2]. The frequency domain methods directly operate on the frequency domain such as: un sharp masking , combining nonlinear low pass and high pass filters, homomorphic filter. As mentioned above, imaging devices apply the power- low transformation on each pixel of the image; hence gamma correction is required to enhance the image. Multimedia data like graphics, audio and video, requires considerable storage capacity and transmission bandwidth. Despite rapid progress in mass-storage density, processor speeds, and digital communication system performance, demand for data storage capacity data-transmission bandwidth continues to outstrip the capabilities of available technologies .The recent growth of data intensive multimedia based web applications has not only sustained the need for more efficient ways to encode signals and images but has made compression of such signals common to storage and communication technology.

A variety of powerful and sophisticated wavelet-based compression schemes[3] for image compression have been developed and implemented[4] . Because of the many advantages, the top contenders in the JPEG-2000 standard are all wavelet based compression algorithms. The wavelet transform has been successfully used in image coding since it allows localization in both the space and frequency domains . Coders can then exploit the characteristics of the wavelet coefficients to achieve better efficiency. Wavelet compression allows the integration of various compression techniques into one algorithm. wavelet-based image coding include Embedded Zero tree Wavelet(EZW)[5] , Set-Partitioning in Hierarchical Trees (SPIHT)[6] , Wavelet Difference Reduction(WDR) , Adaptively Scanned Wavelet Difference Reduction (ASWDR)[7].

In this paper we will have Literature survey of image enhancement methods and wavelet based image compression methods, proposed method, experimental results, statistical analysis of results, finally we will end with our conclusion.

II. BACKGROUND

Before going to details of the method, we present some background topics of image enhancement and image compression which include CLAHE , gamma correction ,wavelet based image compression.

A. Image Enhancement

Image enhancement is the simplest and most appealing areas of digital image processing. Basically, the main idea behind enhancement techniques is to bring out detail that is obscured, or simply to highlight certain features of interest in an image. We have proposed the following CLAHE, gamma correction techniques for enhancing the medical images.

B. Contrast Limited Adaptive Histogram Equalization (CLAHE)

Contrast Limited Adaptive Histogram Equalization differs from ordinary adaptive histogram equalization in its contrast limiting. This feature can also be applied to global histogram equalization, giving rise to contrast limited histogram equalization , which is rarely used in practice. In the case of contrast limited histogram equalization, the contrast limiting procedure has to be applied for each neighbourhood from which a transformation function is derived. contrast limited histogram equalization was developed to prevent the over amplification of noise, which is a problem in adaptive histogram equalization .

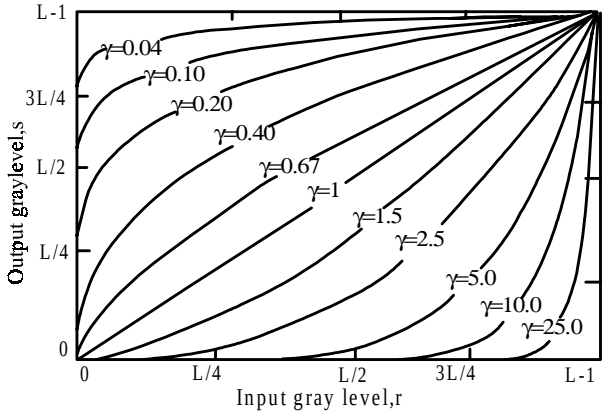

Figure .1 : *Plots of equation* $S = r_C^L$ *for various values of* γ

Plots of s versus r for various values of γ are shown in Figure 1. As in the case of the log transformation, power - law curves with fractional values of γ map a narrow range of dark input values into a wider range of output values, with the opposite being true for higher values of input levels. Unlike the log funciton, however, we notice here a family of possible transformation curves obtained simply by varying γ .

As expected, we see in Figure.1 that curves generated with values of $\gamma > 1$ have exactly the opposite effect as those generated with values of $\gamma < 1$. Finally, we note that Equation (1) reduces to the identity transformation when $c = \gamma = 1$. A variety of devices used for image capture, printing, and display respond according to a power law. By convention, the exponent in the power-law equation is referred to as gamma. The process used to correct this power-law response phenomena is called gamma

correction.

C. Compression

Image compression can be defined as the reduction of the amount of data required to represent a digital image by removing the redundant data. It involves reducing the size of image data files, while retaining necessary information. Wavelet is a mathematical function that divides the data into different frequency components, then fits each component with a resolution suitable for its scale [9]. Wavelet is a waveform that effectively has a duration limit of zero mean value. Some applications that have been successfully realized by utilizing such wavelet are image data compression, watermarking, edge detection, radar systems, and encoding fingerprints.. In fact, there are many coefficients in the representation of wavelet with very small or zero value. This characteristic gives the opportunity to perform image data compression. The application of wavelet transform in digital image processing uses the Discrete Wavelet Transform or DWT.

A variety of sophisticated wavelet-based image coding schemes are Embedded Zero tree Wavelet (EZW) , Set-Partitioning in Hierarchical Trees (SPIHT), Wavelet Difference Reduction(WDR), Adaptively Scanned Wavelet Difference Reduction (ASWDR) etc .

Because of Many advantages of wavelet based image compression as listed below, the top contenders in the JPEG-2000 standard are all wavelet-based compression algorithms.

- Wavelet coding schemes at higher compression avoid blocking artifacts.
- They are better matched to the HVS (Human Visual System) characteristics.
- Compression with wavelets is scalable as the transform process can be applied to an image as many times as wanted and hence very high compression ratios can be achieved.
- Wavelet based compression allow parametric gain control for image softening and sharpening.
- Wavelet-based coding is more robust under transmission and decoding errors, and also facilitates progressive transmission of images.
- Wavelet compression is very efficient at low bit rates.
- Wavelets provide an efficient decomposition of signals prior to compression.

III. PROPOSED WORK

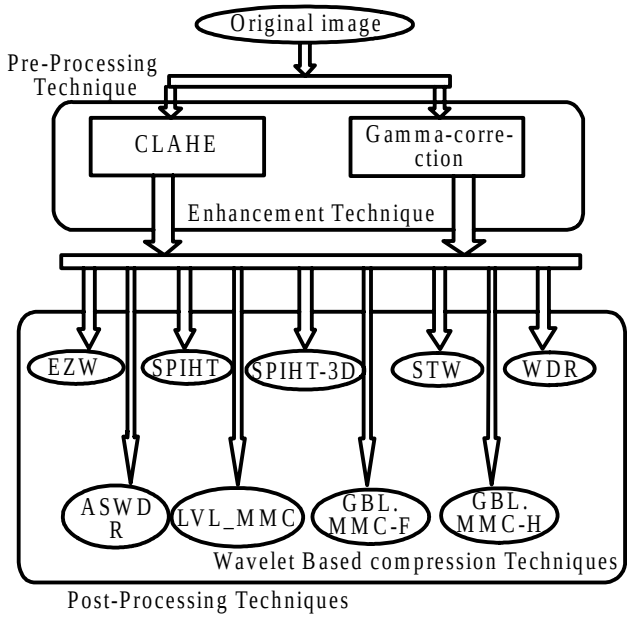

Figure . 2 : *Block Diagram of Proposed work*

The proposed method is used to enhance and compress the medical image. We use the Contrast limited adaptive Histogram Equalization(CLAHE) and Gamma Correction for enhancing the images, and Wavelet based Compression algorithms for compressing the Enhanced medical image.

IV. EXPERIMENTAL RESULTS

Here we can use some medical image modalities like MRI, CT scan, ECG etc. For example here we are using an image which is Coronal image from MRI of the abdomen/ pelvis demonstrating atrophic native kidneys with enhancing solid tumors in both kidneys (here, 2 on the right mid-upper pole and 1 on the left upper pole), the largest measuring 3cm x 2.8cm x 3.2cm.Figure 3 shows experimental results. Figures. 3.a is original image, Figures. 3.b is enhanced image via CLAHE and Figures.2.c is enhanced image via Gamma Correction.Figure.2c. is compressed image.

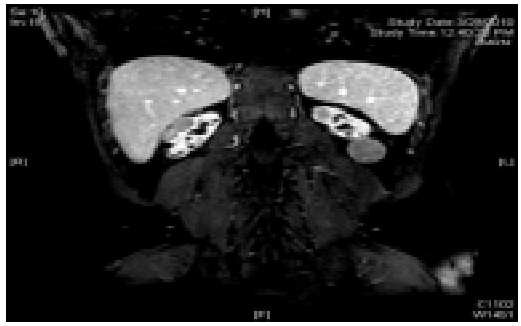

Figure.3(a) *Original MRI Image*

Figure.3 (b) *Enhanced Image by CLAHE*

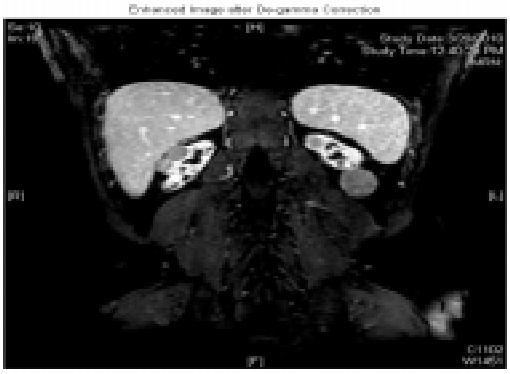

Figure.3 (c) *Enhanced Image by GAMMA CORRECTION*

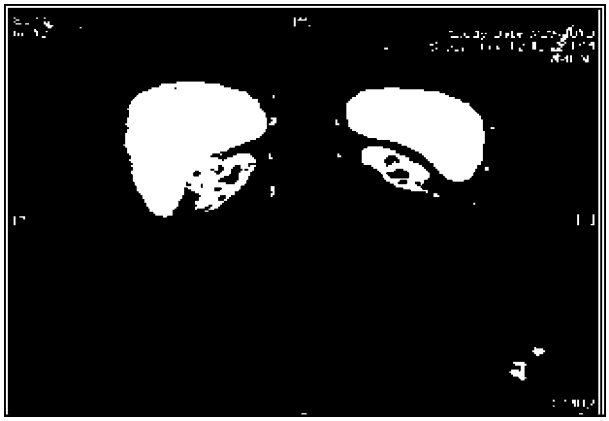

Figure.3(d)Gamma corrected *Compressed Image*

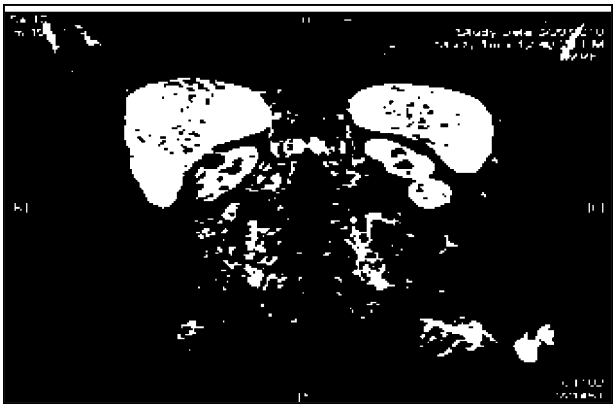

Figure.3(e) CLAHE *Compressed Image*

V. STATISTICAL ANALYSIS

The performance of the proposed method was rigorously evaluated using quality metrics like Compression Ratio (CR), and Peak Signal to Noise Ratio (PSNR)[10],Bits per pixel(BPP),L2-norm.ratio,Max.error,Mean square error.

$$MSE = \sum_{i=1}^{x}\sum_{j=1}^{y}\frac{(|A_{ij} - B_{ij})}{x * y} \quad .....(1)$$

(1) The Peak Signal to Noise Ratio (PSNR) is calculated using the formula MSE: Mean-Square error. x: width of image. y: height. x*y: number of pixels (or quantities).

$$PSNR(dB) = 10 * \log\frac{255^2}{MSE} \quad .....(2)$$

(2) The ratio of the original (uncompressed) image to the compressed image is referred to as the Compression Ratio C_R = (Uncompressed image size) / (compressed image size)

$$C_R = (U_{size})/(C_{size}) \quad .....(3)$$

Where

$$U_{size} = M * N * K \quad .....(4)$$

C_{size} = Size of compressed image file stored in a disk.

(3) Bits per pixel(BPP):Bpp can be defined as

BPP = (no.of encoded bits) / (m*n). .....(5)

Table1: *Quality Assessment metrics for Gamma corrected compressed MRI image*

Comp. method / parameter	EZW	SPIHT	WDR	ASWDR	STW
MSE	11.49	18.1	13.53	12.37	12.37
Max.Err	28	41	38	26	26
L2norm	99.88	98.67	99.29	99.32	99.32
PSNR	37.53	35.55	36.82	37.21	37.21
BPP	2.5857	1.820	2.937	2.830	2.493
C.R	10.77	7.58	12.24	11.79	10.39

Table2: *Quality Assessment metrics for CLAHE compressed MRI image.*

Comp. method / parameter	EZW	SPIHT	WDR	ASWDR	STW
MSE	15.28	25.34	18.58	18.58	16.6
Max.Err	29	39	33	33	26
L2norm	99.89	98.71	99.30	99.30	99.34
PSNR	36.29	34.09	35.44	35.44	35.93
BPP	3.940	2.708	4.656	4.470	4.013
C.R	16.42	11.29	19.40	18.63	16.72

VI. CONCLUSION

In this paper we proposed two image enhancement methods and some wavelet based image compression methods.

By observing all of the above quality assessment metrics for "MRI of Lungs" image, we can conclude that between two enhancement methods "Gamma Correction" method will produce better results than "CLAHE" method.

Among all the compression methods "embedded zero tree wavelet (EZW)" will give good results in case of mean square error(MSE) , peak signal to noise ratio(PSNR),compression ratio(Comp.Ratio) , Max.Error , and "wavelet difference reduction(WDR)" will give good results in case of L2-norm ratio, Bits Per Pixel.

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Plaque Characterization and Segmentation of Coronary Atherosclerosis Images

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ABSTRACT

Vulnerable plaques are lesions presenting high risk of rupture, possibly leading to brain stroke or heart attack. Blood contains lipoproteins, which carries cholesterol and triglycerides. At the time of travelling of lipoporoteins, some of them stick to the walls of the arteries. Low density lipoproteins are "bad cholesterols" that stick to the walls. High density lipoproteins are "good cholesterols" that clean the vessels and transport the cholesterol back to the liver to be metabolized. The "plaque" that sticks to the inside walls of the vessels and narrows the lumen. Plaque is very sticky. Platelets in the blood get trapped on the plaque, causing further narrowing. The blood vessel hardened and possibility of rupture is quite often. Heart attacks are occurred due to High cholesterol, Diabetes, High blood pressure, Smoking, Mental stress, Obesity.

In this project we use intravascular ultrasound (IVUS) technique. It is a catheter based medical imaging technique particularly useful for studying atherosclerotic disease. It produces cross-sectional images of blood vessels that provide quantitative assessment of the vascular wall, information about the nature of atherosclerotic lesions as well as plaque shape and size. Automatic processing of large IVUS data sets represents an important challenge due to ultrasound speckle, catheter artifacts or calcification shadows. In this project we use matlab software.

The aim of the project is to segment different plaques deposited in the interior part of an aorta and to analyze the severity [to classify whether the pathology is Acute or Chronic] of the problem.

In this paper, we present a method for the automatic estimation of the RMM mixture parameters by means of the expectation maximization algorithm, which aims at characterizing tissue echomorphology in ultrasound (US). The performance of the proposed model is evaluated with a database of in vitro intravascular US cases. We show that the mixture coefficients and Rayleigh parameters explicitly derived from the mixture model are able to accurately describe different plaque types and to significantly improve the characterization performance of an already existing methodology.

Index terms

Image segmentation, Intravascular ultrasound (IVUS), Plaque characterization, Rayleigh mixture model (RMM), Vulnerable plaque.

1. INTRODUCTION TO SEGMENTATION

Segmentation is the process of separating a digital image into different regions which have similar properties such as gray level, colour, texture, brightness etc. So that the image can be more understandable and helpful to analyzing. On the basis of pixel intensity we can differentiate the boundaries of different objects. Segmentation identifies separate object within an image and also find boundary between different regions. Segmentation can be classified into two types: local segmentation and global segmentation. Local segmentation is small windows on a whole image and deal with segmenting sub image. Global segmentation deals with segmenting whole image. Global segmentation mostly deals with relatively large no of pixel. But local segmentation deal with lower no of pixel as compare to

global segmentation. Image segmentation is one of the classical problems in image processing and computer vision. Using of Image segmentation we can able to understand the fundamental of digital image processing. Image segmentation is used to enhancement of image and also useful to different medical application. Image segmentation can also use for analysis of the image and further pre-processing of the image. After a segmentation process each phase of image treated differently. Now we are going through about medical images like Ultrasound Images (US) which is widely used today.

Medical images play a vital role in assisting health care providers to access patients for diagnosis and treatment. Studying medical images depends mainly on the visual interpretation of the radiologists. However, this consumes time and usually subjective, depending on the experience of the radiologist. Consequently the use of computer-aided systems becomes very necessary to overcome these limitations. Artificial Intelligence methods such as digital image processing when combined with others like machine learning, fuzzy logic and pattern recognition are so valuable in Image techniques. The computerization of medical image segmentation plays an important role in medical imaging applications. It has found wide application in different areas such as diagnosis, localization of pathology, study of anatomical structure, treatment planning, and computer-integrated surgery. However, the variability and the complexity of the anatomical structures in the human body have resulted in medical image segmentation remaining a hard problem.

INTRODUCTION TO ATHEROSCLEROSIS

Atherosclerosis is a specific form of arteriosclerosis (thickening & hardening of arterial walls) affecting primary the intima of large and medium - sized muscular arteries and is characterized by the presence of fibrofatty plaques. The term atherosclerosis is derived from “athero” referring to the soft lipid - rich material in the centre of atheroma, and “sclerosis” referring to connective tissue in the plaques. Atherosclerosis is often called as arteriosclerosis. Arteriosclerosis can occur in several forms, including atherosclerosis. Atherosclerosis is a heart disease, and is a type of arteriosclerosis or hardening of the arteries. An artery is made up of several layers: an inner lining called the endothelium, an elastic membrane that allows the artery to expand and contract, a layer of smooth muscle, and a layer of connective tissue. Arteriosclerosis is a broad term that includes a hardening of the inner and middle layers of the artery. It can be caused by normal aging, high blood pressure, menta stress, lack of inactivity and by diseases such as diabetes. Atherosclerosis is a type of arteriosclerosis that affects only the inner lining of an artery. It is characterized by plaque deposits that block the flow of blood. Plaque is made of fatty substances, cholesterol, wast products from the cells, calcium, and fibrin, a stringy material that helps clot blood. The plaque formation process stimulates the cells of the artery wall to produce substances that accumulate in the inner layer. Fat builds up within these cells and around them, and they form connective tissue and calcium. The inner layer of the artery wall thickens, the artery’s diameter is reduced, and blood flow and oxygen delivery are decreased. Plaques can rupture, causing the sudden formation of a blood clot (thrombosis). Atherosclerosis can cause a heart attack if it completely blocks the blood flow in the heart (coronary) arteries. It can cause a stroke if it completely blocks the brain (carotid) arteries. Atherosclerosis can also occur in the arteries of the neck, kidneys, thighs, and arms, causing kidney failure or gangrene and amputation.

APPLICATION AREAS OF IMAGE PROCESSING

- Aerospace
- Biometrics
- Medical
- Finance
- Control System
- Signal, Image, Audio and Video
- Neural networks, Fuzzy logic
- Animation

INTRODUCTION TO INTRVASCULAR ULTRASOUND (IVUS)

Vulnerable plaques are lesions presenting high risk of rupture, possibly leading to brain stroke or heart attack [1]. In medical ultrasound (US), a transmitted ultrasonic pulse interacts with an anatomical region providing information about internal tissue structures [2]. The backscattered (received) signal is corrupted by a characteristic granular pattern noise called speckle [3], which depends on the number of scatterers (reflectors) as well as their size. As pointed out in [4], these features can be considered as tissue histological descriptors.

Intravascular US (IVUS) is an imaging technique that allows to clearly assess the arterial wall internal echomorphology. The technical procedure of acquiring IVUS data consists in introducing a catheter, carrying a rotating US emitter inside the vessel. During rotation, a piezoelectric transducer transmits US waves and collects the reflected components that are afterward converted into

electrical signals (A-lines) and sampled by an analog to digital converter. The IVUS image obtained by processing the received echoes is a 360^{o} tomographic view of the inner arterial walls [see Figure 1(a)]. Thus, IVUS is considered a suitable technique for *in vivo* characterization of the coronary plaques composition.

This paper intends to model the atherosclerotic plaque through the analysis of the envelope backscattered IVUS data. For this purpose, an hypothetical model is considered, where a scanned tissue sample suffers from a certain number of scattering phenomena, as depicted in Figure 2.

The most common model for speckle formation, known as fully developed speckle, considers a tissue or region composed of a large number of scatterers, acting as echo reflectors. These scatterers arise from in homogeneity and structures approximately equal to or smaller in size than the wavelength of the US, such as tissue parenchyma, where there are changes in acoustic impedance on a microscopic level within the tissue. It is recognized that under fully developed speckle, pixel intensities in envelope images are well modeled by Rayleigh probability density functions (PDFs) [3], [5]. An application example is given in [6], where the morphological properties of the arterial vessel on IVUS images are modeled by means of a Rayleigh distribution in a fully automatic method for luminal contour segmentation.

Plaque echomorphology may result from different types of components, spatial organization, and complexity, which determine different scattering phenomena, where the Rayleigh distribution would be a reasonable approximation but a compound statistical model would be more appropriate. Hence, the description of tissue echomorphology may be tackled with complex distributions, depending on multiple parameters or with a mixture of simple distributions. Following the latter approach, this paper uses a combination of Rayleigh distributions—Rayleigh mixture model (RMM)—estimated with the expectation maximization (EM) algorithm, thus, making the modeling of tissue echomorphology a rather simple but fast and robust process.

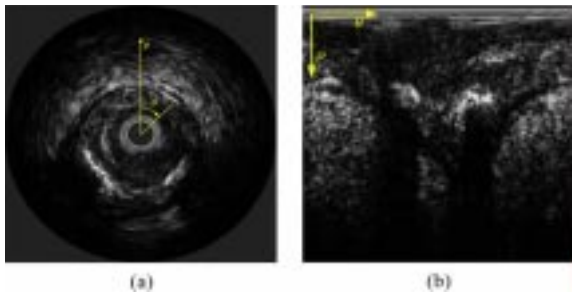

Figure. 1. (a) Cross-sectional Intravascular US (IVUS) image (in cartesian coordinates) and (b) corresponding polar representation; ρ represents the depth in the tissue and θ the position (angle) in the rotation of the probe.

The RMM consists of a technique to describe a particular data distribution by linearly combining different PDFs. Up to our knowledge, the RMM was never used for tissue characterization in US, although, these models have been successfully employed in other fields, such as in underwater acoustics and speech processing problems [11].

The contributions of this paper can be summarized as follows. First, in Section II-A, we provide a comprehensive mathematical formulation of the mixture model, which makes use of the EM algorithm for estimating the coefficients and Rayleigh parameters of the mixture PDF. Second, the adequacy of the proposed model to describe the envelope US data is evaluated using a validated IVUS data set of different plaque types (see Section III). Moreover, the RMM is applied for modeling

Plaques as monolithic objects, i.e., by considering all the pixels enclosed in the plaque. The features explicitly obtained from the mixture model (cf. Section II are used to investigate the discriminative power of the model for identifying different tissue types, namely, fibrotic, lipidic, and calcified tissues. Then, in Section III, the ability of the RMM for pixel wise classification of plaque composition is evaluated when using only the new features and when combining them with other texture and spectral features recently proposed [12]. Finally, we investigate the significance of the obtained classification improvement when using the RMM features .

II. METHODS

This section aims at providing the mathematical description for estimating the mixture coefficients (weights) and the Rayleigh parameters associated with each mixture component (distribution) using the EM method applied to US data.

A. Rayleigh Mixture Model

Let $Y = \{y_i\}, 1 \le i \le N$, be a set of pixel intensities of a given region of interest (plaque) from an US image. Pixel intensities are considered random variables, which are described by the following mixture of L distributions:

$$p(y_i \mid \Psi) = \sum_{j=1}^{L} \theta_j p(y_i \mid \sigma_j) \qquad \text{.....(1)}$$

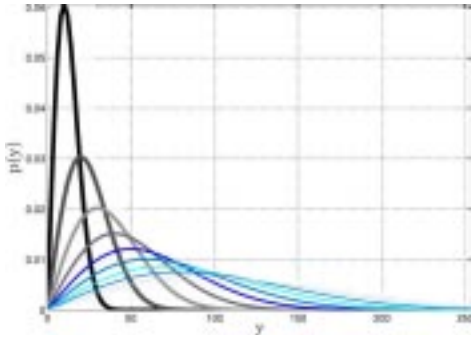

Figure. 2 : *Rayleigh PDFs generated with parameter*

where σ_j is the parameter of the Rayleigh PDF $p(y_i \mid \sigma_j)$ given by

$$p(y_i \mid \sigma_j) = \frac{y_i}{\sigma_j^2} e^{-\frac{y_i^2}{2\sigma_j^2}} \quad \text{.....(2)}$$

and the parameters $\Psi = (\theta_1,....,\theta_L,\sigma_1,...\sigma_L)$ are the coefficients (θ_j) and Rayleigh parameters (σ_j) of the mixture, respectively. The condition $\sum_{j=1}^{L}\theta_j = 1$ must hold to guarantee that $p(y_i \mid \Psi)$ is a true distribution function.

The parameters σ_j associated with the pixel intensity y_i characterize the acoustic properties of the tissue at the ith location [13]. The effect changing σ in the shape of the distribution and thus in th eimage intesity is illustrated in Figure 2. The joint distribution of the pixel intensities, considered independent and identically distributed (i.i.d), is given by

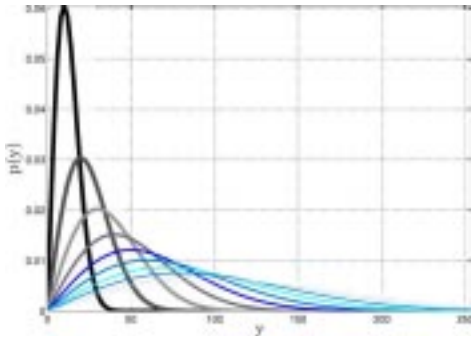

Figure. 2 : *Rayleigh PDFs generated with parameter* $10^2 < \sigma < 10^3$ *(from darker to lighter curves).*

$$p(Y \mid \Psi) = \Pi_i^N p(y_i \mid \Psi) \quad \text{.....(3)}$$

The goal is to estimate Ψ by maximizing the likelihood function such that

$$\overline{\Psi}_{ML} = \arg\max_{\Psi} L(Y,\Psi) \quad \text{.....(4)}$$

Where

$$L(Y,\Psi) = \log(Y \mid \Psi) = \sum_{i=1}^{N}\log\left(\sum_{j=1}^{L}\theta_j p_j(y_i\sigma_j)\right) \text{(5)}$$

The maximization of (5) is a difficult task because it consists of a logarithmic function of a sum of terms. To overcome this difficulty, the EM [14] method is used, where a set of hidden variables are introduced, $\{K = k_i\}$ with $K_i \in \{1,....,L\}$. The value of $K_i = j$ informs us about the mixture component j that generated the ith pixel intensity y_i, with probability $p(y_i \mid \sigma_{ki})$ defined in (2). Each nth iteration of the EM method is composed of two steps:

1) E step: where the expectation of the new likelihood function $L(Y,K,\Psi)$ is computed with respect to K

$$Q(Y,\Psi^n,\Psi) = E_k[L(Y,K(\Psi_n,\Psi))] \text{(6)}$$

2) M step: where a new estimate of Ψ, Ψ^{n+1} is obtained by maximizing the function Q

$$\Psi^{n+1} = \arg\max_{\Psi} Q(Y,\Psi^n,\Psi) \text{(7)}$$

These two steps alternate until convergence is achieved.

B. RMM Features

The technique for estimating the RMM parameters and coefficients using the EM method has been presented. We are further interested in assessing the adequacy of the proposed model to describe different types of tissue, and particularly, to characterize the atherosclerotic plaque.

III. EXPERIMENTAL RESULTS

In this section, we first provide a description of the methods used to acquire and process the IVUS data, and we briefly introduce the classification framework adopted for tuning the RMM algorithm and performing plaque characterization. Then, two distinct experiments are conducted: the first studies the adequacy of the RMM for describing different tissue types. This experiment is designated as monolithic description since the mixture model is estimated by considering all the pixels enclosed in the plaque. The second experiment refers to plaque characterization made pixel-by-pixel (hence, called plaque local characterization), where the RMM is applied not to the entire plaque, but to each processing block centered at

the pixel to be characterized. Given this, the ability of the RMM for local characterization of plaque composition is evaluated when using only the RMM features and when combining them with other texture and spectral features Finally, we present a statistical analysis that supports the relevance of the obtained classification improvement when using the RMM features.

A. In Vitro Data Processing

The adequacy of the proposed RMM to describe real tissue types is evaluated through an *in vitro* study of atherosclerotic plaques from an IVUS database. The IVUS data set has been recently presented in [12] and consists of eight postmortem arteries, resulting in 45 frames with 24 fibrotic, 12 lipidic, and 31calcified plaques. This data set, composed of 67 plaques, has been validated by histological analysis.

The information encoded in the visual appearance of tissues naturally represents a relevant feature for their description. However, during acquisition, the imaging parameters of the IVUS equipment are typically changed to enhance tissue visualization. Hence, parameters like contrast depth and brightness can change from patient to patient or even from image to image. When the IVUS images are then processed for feature extraction, this fact may generate non comparable features.

To avoid the aforementioned errors and to produce normalized data, the used data follows a rigorous acquisition protocol, where the IVUS images have been directly reconstructed from the raw RF signals, rather than using the ones produced by the IVUS equipment. For this purpose, we follow an image reconstruction algorithm outlined in Figure 3.

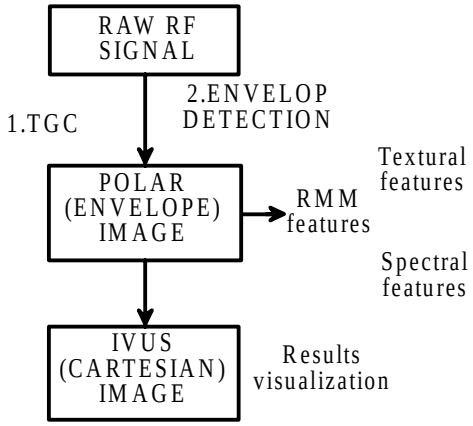

Figure 3 : *IVUS data processing (see text for details). RMM, textural, and spectral features are extracted from polar image.*

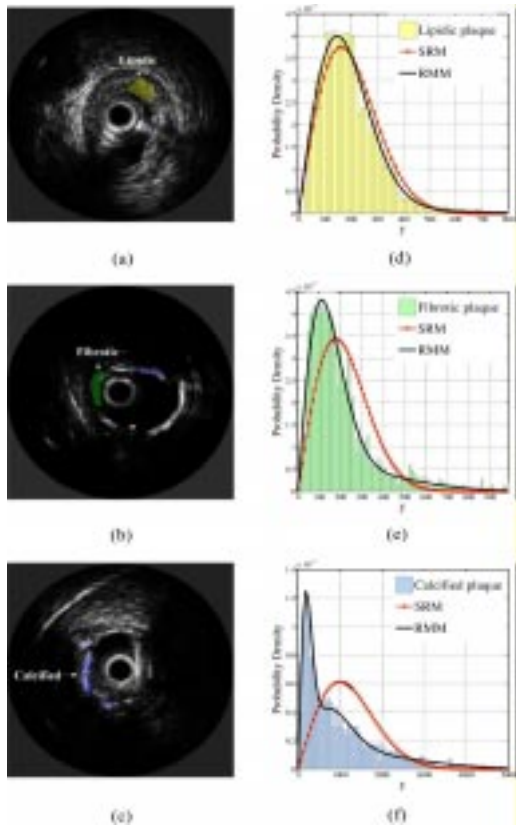

Figure. 4 : *(a)–(c) RMM modeling of three tissue types. (d)–(f) three-component mixture PDFs estimated for each tissue type, overlapped with single Rayleigh PDFs.*

B. Classification Framework

As stated previously, the weights and parameters of the mixture distribution, whose estimation was early described, are used as features to describe different types of plaque. In order to evaluate the correct modeling, we adopt a multiclass classification framework that has been successfully used in plaque characterization [12].

The role of the classification scheme is twofold:

1) It allows to evaluate the discriminative power of RMM features; and 2) it is used to support a cross-validation process, adopted to tune the L parameter (number of mixture components) in RMM model and the kernel size (image window size, where the RMM is estimated).

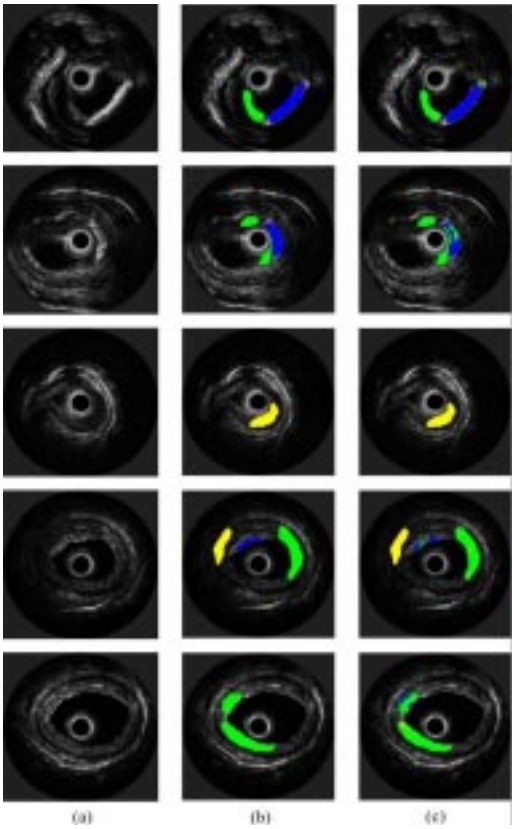

Figure 5 : *Examples of plaque classification (a) IVUS images, (b) ground truth images, segmented according to the histological analysis, (c) classification. In blue (dark), green (mid gray), and yellow (light gray) are indicated calcified, fibrotic, and lipidic tissues, respectively.*

CONCLUSION

In this paper we present the segmentation of plaque characterization in IVUS data based on a mixture of rayleigh distributions and we analyze the severity of the problem.

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A Survey on Copy Move Forgery Detection Techniques

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ABSTRACT

Digital images are a powerful tool of communication medium now a days. Image authenticity is very much important because it is going to be used in many areas such as law firms, medical sciences, media etc. as a proof. But due to the advanced technologies available now it's very easy to manipulate the image which is termed as forgery. Copy move forgery is the type of image forgery in which one part of the image is hidden by covering with some other part of the same image. This copy move forgery detection is one of the most progressive research topic now a days. Several algorithms to detect this type of forgery have been proposed. In this paper evaluation of the performance of different techniques to detect copy move forgery is done by considering different metrics.

Index Terms

forgery, tool, progressive research, metrics. (Key words)

I. INTRODUCTION

From past few decades images have become the proof of occurrence of the events in life. Due to the diversific-ation of use of computers in different fields of modern life has given a very much importance to the digital images. Low cost and great availabilities of hardware and software tools made the image operations such as creating, editing and manipulating the images more easy now a days. Hence to consider the image as a proof or evidence is not justifiable. The authenticity of digital images has now become volatile. This situation made it questionable the use digital images as a proof in law, in forensic science, in sports, in news and in business etc. Hence the detection of forgeries in digital images has become an emerging research topic now a days. Copy move image forgery is the type of image forgery in which both the source and target regions are from the same image, hence both the parts contains same values for properties such as brightness, illumination etc. the forgery detection in digital images are broadly classified in to two types namely active approaches and passive approaches. Active approaches are digital image water-marking and signature analysis.

Both these techniques require an external input to be verified. This method is not very much suited for all types of images because there are so many images in internet available without any signature incurred in it. Passive approaches are much suitable to these type of images because they doesn't require any external input except input required to detect the forgery in images. There are three techniques widely used in manipulating the digital image. They are image retouching, image slicing and copy move forgery. Image retouching doesn't alter the major portion of the image. Image splicing is the process of adding two different images to create a new image. Currently in this paper we are discussing about detection of copy move forgery.

II. COPY-MOVE FORGERY

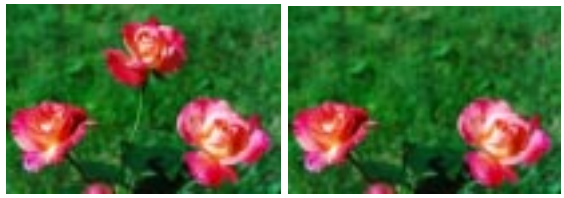

Figure 1(a): *Original Image*

Figure 1(b): *Tampered Image*

Copy move forgery is the type of image forgery in which a part of the image is overridden by some another part of the same image. Here both the source and target part of the image are parts of the same image. The example of copy move image forgery is shown in the below Figure.

In the above Figure, Figure (a) is the original image and the Figure (b) is the tampered image .in Figure (b) the top middle flower is covered by the greenery in the image. Copy-Move forgery is performed with the intention to make

an object "disappear" from the image by covering it with a small block copied from another part of the same image. Since the copied segments come from the same image, the color palette, noise components, dynamic range and the other properties will be compatible with the rest of the image, thus it is very difficult for a human eye to detect. There are many approaches are proposed to detect the copy move forgery in digital images. One of the simplest approach is performing exhaustive search.

In this approach the image is overlaid by its circularly shifted version and search for approximate matching parts of image is done. This method is simple and more suitable for small images. For an image with dimensions (M x N) it will take $(MN)^2$ steps to complete the testing. Hence this method is computationally expensive for medium and large dimensional images. Other technique used is autocorrelation for copy move forgery. Since the forged part of the image is also from the same image there is a correlation between original and duplicated regions. Although this method is simple practically it fails in detection of copy move forgery.

III. BLOCK-BASED ALGORITHMS

Now other approach for detecting copy move forgery is block matching procedure. Here in this approach the image is divided into overlapping blocks and each block is compared based on some of the features extracted from it with the remaining. The idea here is to detect connected blocks that are copied and moved. The copied region would consist many overlapping blocks. The distance between each duplicated block pair would be same since each block are moved with same amount of shift. The next step is to extract the feature from each block. Here the duplicated block and source block will have almost similar values of the features then the extracted features are vectorised and placed in a matrix. This matrix is lexicographically sorted and then the vectors with almost similar values are grouped together, which represents the copied and moved blocks in the image. This block matching procedure is explained as below.

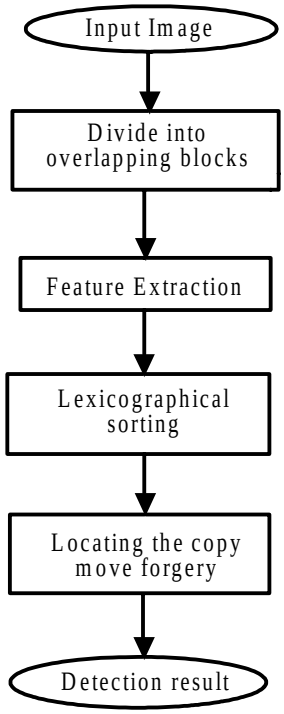

Figure 2 : *Block matching procedure*

The Feature Extraction methods using block-based approach are mainly categorized in to four categories. They are dimensionality reduction based, and frequency domain-based, intensity-based and moment based features.

A. Dimensionality reduction-based

Dimensionality reduction based methods uses PCA (Principle Component Analysis) and KPCA (Kernel-PCA). Computed the singular values of a reduced-rank approximation (SVD).

B. PCA and KPCA

PCA is a method that projects a dataset to a new coordinate system by determining the eigenvectors and eigenvalues of a matrix. It involves calculation of covariance matrix of a dataset to minimize the redundancy and maximize the variance. The PCA is computed by determining the eigenvectors and eigen values of the covariance matrix. The covariance matrix is used to measure how much the dimensions vary from the mean with respect to each other. The covariance of two random variables (dimensions) is their tendency to vary together as:

$$Cov(X,Y) = E[E[X]-X].E[E[Y]-Y] \quad .....(1)$$

Where E[X] and E[Y] denote the expected value of X and Y respectively.

KPCA (Kernel-PCA) proposed by Bashar *et al.* Kang *et al.* Kernel PCA (KPCA) was derived from PCA as a nonlinear feature extraction method, Theoretically, KPCA may be viewed as a combination of the following

two procedures: the first procedure implicitly transforms the input space into a higher-dimensional feature space, and the second one carries out PCA in the feature space. By virtue of so-called kernel functions, KPCA is computationally tractable compared to other nonlinear methods.

C. Intensity-based

The intensity based feature extraction approach used to perform the average of red, green and blue components generally. Additionally dimensional information of blocks (LUO) method is proposed by Luo *et al.* Bravo-Solorio *et al., proposed a method which calculate the* entropy of a block as a discriminating feature (BRAVO). Lin *et al.* (LIN) computed the average grayscale intensities of a block and its sub-blocks. Wang *et al.* used the mean intensities of circles with different radii around the block center (CIRCLE).

D. Frequency based

Frequency based algorithms uses DCT, DWT and FMT to perform feature extraction. They are explained briefly below.

1) **DCT :** Fridrich *et al.,* proposed the use of 256 coefficients of the discrete cosine transform (DCT) as features [1]. , the Discrete Cosine Transform (DCT) attempts to decorrelate the image data. After decorrelation each transform coefficient can be encoded independently without losing the Compression efficiency. Decorrelation, Energy Compaction, seperability and symmetry are the four distinct properties of the DCT that makes the feature extraction more efficient. The 2-D DCT functions which can be applied to image are given by,

Forward transform

$$X(m,n)=u(m)u(n)\frac{2}{N}\sum_{i=0}^{M-1}\sum_{j=0}^{N-1}x(i,j)\cos\frac{(2i+1)m\pi}{2M}\cos\frac{(2J+1)n\pi}{2N}$$

For m = 0,1,….,M-1,n-0,1,…,N-1. .....(2)

Inverse transform

$$x(i,j)=\frac{2}{N}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}x(m)u(n)X(m.n)\cos\frac{(2i+1)m\pi}{2M}\cos\frac{(2j+1)n\pi}{2N}$$

for i = 0,1,…,M-1,j = 0,1,…,N-1 .....(3)

Where X (m, n) are the DCT Coefficients and x(i,j) are the image samples in block. Here we consider the image size as MxN.

The discrete cosine transform is calculated for each block and stored in a row of matrix which contains the coordinates of the block starting point at the end of the row. Then this matrix is sorted lexicographically and the rows which are having same values are treated as copied regions and those blocks are highlighted as forged parts.

2) **DWT :** The coefficients of a discrete wavelet transform (DWT) using Haar-Wavelets were proposed as features by Bashar *et al.* [3]the wavelet transform gives the analysis of the data both in time as well as frequency domains. The technique proposed by Jing Zhang et al [9] works by applying DWT to input image to yield a reduced dimension representation. Then the phase correlation is computed to estimate the spatial offset between the copied region and the pasted region. The copy-move regions can then be located by the idea of pixel matching, which is shifting the input image according to the spatial offset and calculating the difference between image and its shifted version.

The DWT transform also reduces the dimensionality of the image based on the scaling factor we consider. This will gives a better performance in data compression. The DWT used to project the image in to frequency domain and the sub-band which contains maximum information is selected (most likely LL sub-band) and then these values are stored in a matrix and that matrix is lexicographically sorted and the rows with similar values are get traced and the blocks of image corresponds to that rows are considered as the forged parts of the image.

3) **FMT :** Bayram et. al [8] suggested a method by applying Fourier Mellin Transform (FMT) on the image block. They first obtained the Fourier transform representation of each block, re-sampled the resulting magnitude values into log-polar coordinates. Then they obtained a vector representation by projecting log-polar values onto 1-D and used these representations as our features.

E. Moment based

1) **Blur invariant moments:** These moments are proposed by Mahdian and Saic.[8] This method used to identify the copied part even though it is blurred to isolate the edge discontinuities. Generally, relation between the ideal image f and the observed image g is described as where D is a degradation operator. In the case of a linear shift-invariant imaging system, D usually has a form of

$$g=\tau(f)*h+n \qquad .....(4)$$

where h is the point-spread function (PSF) of the system, n is an additive random noise. We want to define a function which again reproduces f from g. That type of function is applied to each and every block and the coefficients are stored in a matrix and comparison of the

so obtained values is done to find out the copied and forged parts of the image.

2) **Zernike moments:** Ryu *et al* [9] proposed the use of Zernike moments. These Zernike moments are the rotation invariant moments which are having the same value even if the image is rotated to a particular angle.

IV. KEY POINT-BASED ALGORITHMS

Unlike block-based algorithms, key point-based methods rely on the identification and selection of high-entropy image regions (i.e. the "key points"). A feature vector is then extracted per key point. Consequently, fewer feature vectors are estimated, resulting in reduced computational complexity of feature matching and post-processing. The lower number of feature vectors dictates that post processing thresholds are also to be lower than that of block-based methods. A drawback of key point methods is that copied regions are often only sparsely covered by matched key points. If the copied regions exhibit little structure, it may happen that the region is completely missed. We examined two different versions of key point based feature vectors. One uses the SIFT features while the other uses the SURF features they are denoted as SIFT and SURF, respectively [4][7]. Comparison of different algorithms based on feature vector length is done in below table.

SIFT : The SIFT approach, for image feature generation, takes an image and transforms it into a "large collection of local feature vectors" the f local features extracted through the following three stages, explained here shortly

TABLE I

COMPARISON OF DIFFERENT ALGORITHMS

GROUP	Methods	Feature vector length
Moments	BLUR	24
	HU	5
	ZERNIKE	12
Dimensionality reduction	PCA	-
	SVD	-
	KPCA	192
Intensity	LUO	7
	BRAVO	4
	LIN	9
	CIRCLE	8
Frequency	DCT	256
	DWT	256
	FMT	45
Key point	SIFT	128
	SURF	64

Here by analyzing the Figure (2) and Figure (3) we notice that the DCT and DWT methods have highest length of feature vector followed by KPCA. The larger the length of feature vector the more accurate detection capability the method have. But it has the time limitation since having larger feature vector length will take more time for detection.

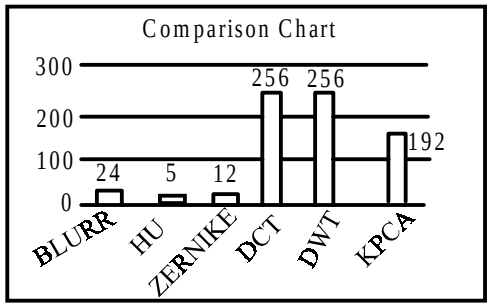

Figure (3): *Chart comparison of different algorithms*

V. CONCLUSION

In this paper we reviewed several papers to know the recent development in the field of Copy-Move digital image forgery detection. All the methods which have been suggested draw strengths from different transforms to make them robust against post processing and to reduce the number of logical blocks to compare. Different feature extraction techniques which provides the detection capability of different moves to hide the forgery are discussed. DCT, DWT and FMT are frequency domain feature extraction techniques. In these methods feature extraction is done by using 2-D forward transforms and the feature vectors are calculated. The FMT algorithms works for the case of only slight rotation. Blur invariant moments and Zernike moments are the blur and rotation invariant feature extraction techniques. The above mentioned techniques are block matching techniques. Also selection of block size poses problem, Two Key point based methods are also proposed, they are SIFT and SURF. Applied these techniques on forged images and the results are recorded for the purpose of evaluating which technique works better for which type of image. These different methods proposed diversify the process of forgery detection in digital images. Sophisticated tools and advanced manipulation techniques have made forgery detection a challenging one. Digital image forensic is still a growing area and lot of research needed to be done.

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Video Denoising By Robust Temporal Spatial Decomposition

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ABSTRACT

with the advancement in sensor design, the image/video processing became one of the most important issue as most of them one using online videos, editing 2D, 3D videos. Capturing videos for cameras etc. video processing is permanently done by assuming video sequences. Which comes of sequence of frames/images. Video information is reserved in terms of space and time. The information corresponding to space is called spatial information and this is explained in spatial coordinates and information which is represented as a function of time is known as temporal and together called as spatiotemporal respectively. Video processing is easy while video is analyzed and processed in spatiotemporal representation.

The video frames contain noise part.

The extended method for the elimination of noise have some disadvantages like they need fixed sizes for grouping block of objects this makes computational complements and adjustments in that methods gives poor result. Video demising at effectively to remove noise from all the frames of the video by utilizing information in both spatial and temporal domains and one of the method is robust temporal spatial decomposition model which decomposes a video into 3 parts. The temporal spatially correlated part. Future compensation part and sparse noise part. Compared to the existed transform based techniques. This RTSD model mainly lies in robustness. Robustness of RTSD model seek to obtain two major reasons.1) RTSD model is robust to noise.2) RTSD model can be implemented to accommodate background variation to some extent.

While decomposing into 3 parts the video frames may have a high correlation between adjacent frames which leads to low rank matrix and it is corresponded to temporal. Spatial correlated part. To overcome decomposition problem a minimization of convex which models nuclear norm, total variable norm and norm and to solve decomposition problem development of two stage method is done.

Decomposition of total frames into temporal spatially correlated part and residuals. This remaining part which is a combination of frames and future information is further derived into two parts as space noise part and future interaction part separately.

INTRODUCTION

In Video processing sparse representation means among all the coefficients of base vectors only a small fraction of the entries are non-zeros. This representation will select the subset of base vectors which express the input signal most concentrated and automatically reject other less concentrated representations.so sparse representation is used to perform classification task. Sparsely is required for compressing data, feature extraction, detection, image restoration etc.. Sparse representation is done via l1minimization.

In video processing on one hand we extract temporal and spatial correlations from a video sequence and on the other hand, since contents of two adjacent frames generally change little (i.e. The stationary or slowly changing background with foreground moving not too fast usually dominates in consecutive video frames), we are

able to find high temporal correlation between neighboring frames. We define a *"video sequence"* as a 3-D video data cube with high temporal correlation, consisting of several consecutive frames while including no significant scene change. On the other hand, it is obvious that there exists high spatial correlation between neighboring pixels in every frame. We should deal with temporal and spatial correlations togerthly for extracting the correlated component. After removing the part with high temporal and spatial correlations, we get the residual, which captures features such as object movements or lighting variations, still preserves some spatial correlation while is nearly temporally uncorrelated. We can decompose the frames of the whole video sequence into three parts: 1) the temporal spatially correlated part among all frames; 2) the feature compensation part belonging to each frame exclusively; 3) the sparse noise part.

The first part contains most information of the original video frames. The second part, corresponding to the feature part shows significance for capturing the frame's unique characteristic. The sparse noise part, including noise or other common degradations, possesses neither temporal nor spatial correlation.

Robust Principal Component Analysis (RPCA) is the most relevant advanced work in our project. RPCA approximates the temporally correlated component with a low-dimensional subspace, and prove that it can be exactly recovered from sparse outliers with high robustness. Based on the ideas similar to RPCA, a recent work on video denoising reformulates the problem of removing mixed noise as a low-rank matrix completion problem by grouping similar patches in both space and time domains. Its robustness and effectiveness compare favorably against a few state-of-the art denoising algorithms. However, the method potentially suffers from the problem of mismatching as most popular motion compensation based methods do, and its performance highly depends on the accuracy of outlier identification in preprocessing.

OUR CONTRIBUTION

In this paper we develop a robust temporal-spatial decomposition (RTSD) model, which decomposes one video sequence into three parts: the temporalspatially correlated part, the feature compensation part, and the sparse noise part. RTSD models main characteristics and advantages can be summarized as two folds:

1) Compared to the traditional pixel-domain methods, our proposed model analyzes temporal and spatial correlations from a global point of view. In the RTSD model, one video sequence is temporally viewed and decomposed as a 3-D data cube, by which temporal correlation, embedded in not only neighboring frames but also far away frames, can be extracted as a whole. As for each frame, RTSD model processes one frame integrally in space domain as well, thereby effectively preserves spatial correlation during decomposition.

2) Compared to the transform-based techniques, the superiority of RTSD model mainly lies in robustness. The robustness of RTSD model is claimed for two major reasons. Firstly, it should be emphasized that the RTSD model is robust to noise, especially sparse outliers, and can distinguish noise from high-frequency features effectively according to spatial distribution characteristics. Secondly, we need to point out that by choosing proper solving strategies, RTSD model can be implemented to accommodate background variations to some extent.

In addition, we formulate the temporal-spatial decomposition problem as the minimization of a convex function, which consists of a nuclear norm, a TV (total variation)-like norm, and a $l1$ norm. To solve the RTSD model, we develop a two stage method and discuss the solving strategy for each stage in detail. Furthermore, we apply our proposed RTSD model in two video processing applications, e.g., video denoising and scratch detection.

NOTATIONS

Let us consider a video sequence with N frames, denoted as $\tilde{\mathbf{M}}(1)$, …, $\tilde{\mathbf{M}}(N)$, where the ith frame $\tilde{\mathbf{M}}(i)$ *2* $RK1 \times K2$. For the sake of simplicity, each frame is reshaped as a column vector, for example, $\tilde{\mathbf{M}}(i)$ is reshaped as $\mathbf{m}(i)$ *2* $RK1K2 \times 1$. These vectors are combined into a matrix $\mathbf{M}$ *2* $RK1K2 \times N$, with $\mathbf{m}(i)$ being the ith column. We will decompose $\mathbf{M}$ into three parts: the temporal-spatially correlated part $\mathbf{L}$, the feature compensation part $\mathbf{S}1$, and the sparse noise part $\mathbf{S}2$, where $\mathbf{L}$, $\mathbf{S}1$, $\mathbf{S}2$ *2* $RK1K2 \times N$.

In this paper, we will use several matrix and vector norms, defined as follows:

1) The TV (Total Variation) norm. For a 2D matrix $\mathbf{U}$ with u_{jk} denoting its entry on the jth row and the kth column, the TV norm is defined as:

$$\| U \|_{TV} = \sum_j \sum_k \sqrt{\left(u_{j,k} - u_{j-1,k}\right)^2 + \left(u_{j,k} - u_{j,k-1}\right)^2}$$

2) The STV (Separable TV) norm. In order to facilitate further discussions, we define a new separable TV norm, denoted as STV, for the matrix $\mathbf{M}$:

$$\| M \| STV \sum \sum_{i=1} \| = M\tilde{}(i) \| TV$$

Note that **M** is constructed from the video frames,

$\| M \|_{STV}$ indeed represents the sum of the TV norms of all frames. Since the TV norm describes the local smoothness of one frame, the STV norm is hence an indicator of the overall smoothness of all frames.

3) The ℓ_1 norm. For a 1D vector **x** with x_l denoting its l^{th} element, the ℓ_1 norm of **x** is:

$$\| x \|_1 \sum = x_{|l|.1}$$

By a slight abuse of notation, we also define the $?_1$ norm for the 2D matrix **M**:

$$\| M \|_1 = \sum_{i=1}^{N} \| m(i) \|_1 .$$

4) The ℓ_2 norm. The ℓ_2 norm of the 1D vector x is:

$$\| x \|_2 = \sqrt{\sum_l x_l^2}$$

Similarly, we define the ℓ_2 norm (indeed the Frobenius Norm) for the 2D matric M:

$$\| M \|_F = \sqrt{\sum_{i=1}^{N} \| m(i) \|_2^2}$$

5) The nuclear norm. the nuclear norm of the 2D matrix M, is:

$$\| M \|_* = \text{Trace}\left(\sqrt{M^T M} \right)$$

Here λ, μ and γ are user-defined nonnegative constants to balance the three parts.

Problem formulation and solution overview

A problem is occered at temporal spatial decomposition and this is overcomed by minimization of convex function and the decomposition is done in two stages for sub optimal solutions.The video is taken as 2D matrix.A high correlation between adjacent frames leads to low rank matrix „ L _11.The remaining part is S.where S = M-L

Stage1-decomposition: In first stage decomposing entire matrix into separate temporal-spatially correlated part (L) and residual(S).

For this least square (LS): Least absolute deviation (LAD) and robust PCA (RPCA) methods are used for the decomposition of low rank

component from matrix „M_1

Stage2-Decompositon: In second stage of decomposition in the residual (S) into feature compensation part (S1) and sparse noise part (S2).This is done by solving TV-l1 minimization and log-TV l1 minimization. Thus the noise is removed by using Adaptive center-weighted median filter (ACWMF).

1) **The LS approach :** One simplest approach to obtain **L** with rank 1 is to solve the following LS problem: Here **l**(*i*) denotes the *i*th column of **L**. Apparently, the optimal solution to which averages the *N* frames. If the video frames have a static background and the foreground objects changing over a period of time, then most background information is expected to be retained in **L***LS*. On the other hand, feature information uniquely belonging to some frames, such as motions or lighting variations, is to be largely weakened in **L***LS*.

2) **The LAD approach :** Another way to solve a rank 1 component **L** is the LAD method, which is similar to the LS approach but instead minimizes the $\ell 1$ norm of the residuals to enhance the sparsity of residual: The LAD problem (6) can be re-formulated into a standard linear program and solved.

3) **The RPCA approach :** The RPCA approach is basically to solve the following nuclear- $\ell 1$ minimization problem: Here λ'is a user-defined nonnegative constant. By choosing the value of λ', we are able to control the rank of **L**. Here the nuclear norm *j*is a convex approximation to the rank Of **L**. In video processing scenarios, the setting of λ' reflects our estimate on the temporal correlation of video frames. Note that if λ' is properly chosen such that the resulting **L** is with rank 1, RPCA is equivalent to LAD. Though the RPCA problem in (7) is a convex program, solving it is a nontrivial task due to the complicated nuclear norm term. Several algorithms have been developed for the RPCA problem, such as the singular value thresholding method the accelerated proximal gradient method [29], the augmented Lagrangian method (ALM) [30], and the alternating direction method (ADM) [31]. In this paper, we adopt the algorithm based on the (inexact) ADM.

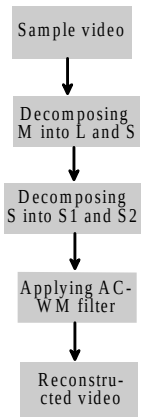
4) **Comparison among LS, LAD and RPCA:** All the three methods introduced above are capable of decomposing a low rank component **L** from a given matrix **M**. We recognize that there are possibly more alternatives that can full fill the task as Stage I of our RTSD model. Here is a brief comparison among LS, LAD and RPCA

Rank of L : LS and LAD both require **L** being exactly rank-1, whereas RPCA permits the rank to be adjusted by properly selecting λ'.Thus if a rank-1 **L** is strictly demanded, e.g., extracting a completely static background

from video surveillance sequences, LS and LAD can be superior choices to RPCA. But it is usually not the case in most video applications. For a practical video sequence whose background can contain mild movement as well, an **L** component with a fixed rank 1 may not offer enough degrees of freedom to describe those important features in background, such as motions or Lighting variations. That is why the LS and LAD approaches are very sensitive to background variations. An adjustable rank of **L** provided by RPCA may be more flexible for describing the common components across a video sequence with background changes.

Complexity: The LS approach is simple and fast, only to average all the frames with linear time complexity. LAD can be re-formulated into a linear program and also enjoys the benefit of fast computation. But for RPCA, since the nuclear norm is nontrivial to handle, its computational complexity is relatively high even with the efficient ADM algorithm [31]. Although the convergence rate of the ADM method for solving (7) is not theoretically specified, extensive numerical experiments have shown that it converges Q-linearly [30], [31]. In each iteration, a singular value decomposition (SVD) step to update **L** accounts for the majority of the computational load; for $L_2R^{K1K2\times N}$, the time complexity of SVD is $O(K1K2N2)$ [32]. Therefore, if high processing efficiency is greatly desirable, e.g., in video coding and other low-delay processing cases, we may prefer the LS and LAD approaches.

Algorithm



M = Total video in matrix,

S = Residual,

L = Temporal spatially correlated part,

S1 = Feature compensation part,

A. The Stage I decomposition

We compare the alternative approach to stage I decomposition as discussed in section 3.1. the simulations are performed on two video sequences, "Paris" (352×288) and "Ferman" (352×288).The "Paris" sequence has a static background, while there is mild transition in the background of the "Ferman" sequence caused by camera rotation and shaking. 90 consecutive frames are extracted from the both sequences. For each, we randomly choose 20% pixels among the sequence and replace their values with noise whose intensity is of uniform distribution between [0,255]. We vectorize the 90 frames and recombine then as one matrix M (101376×90), then apply LS, LAD and RPACA to decompose it into L and S, respectively. The parameter λ'is set to $1/\sqrt{(352\times288)}$, as recommended in [23]. For each sequence, we pick the first original frame M(1), and the corresponding low rank parts (reshaped from the 1st column in L to the original frame size (352×288) obtained by LS, LAD and RPCA approaches, respectively, and compared result in figure 1. For the "Paris" sequence, Figure 1. (b)-(d) show that the temporal-spatially correlated part generated by LAD and RPCA both achieve good visual quality under noise. Through the LS method keeps the fastest running speed, it seems that its low-rank part contains severe blurry artifacts and damaged details in the noisy case, since the information of sparse (impulse) noise on pixels cannot be completely offset.

Fig.1. *Results on "Pairs" and "Foreman"*

For the "Foremen" sequence, however, LAD fails to give a result comparable to RPCA. The sharp performance contracts result from the differences between the two sequences. The first "Paris" sequence keeps a stationary background while the second "Foreman" sequence's background contains certain movements. Because LAD keeps a common part of strictly rank-1, as stated in 3.1.2, it lacks degrees of freedom to describe even slight changes in background. Indeed, background variations appear inevitably in most practical videos, thus to pursue an exactly rank-1 L part may often be unnecessary or impossible. For RPCA, through the rank of L can be varied over different cases, it keeps (relatively) low-rank, and most sequences, at the top and bottom rows, respectively. Sequences, at the top and bottom rows, respectively. In each row, the original frame and the corresponding low-rank part in L decomposed by LS, LAD and RPCA are listed in a left-or-right order. About the L part decomposed by RPCA, its rank in 41 for "Paris" sequence, and 45 for "Forman" sequence.

B. The Stage II decomposition

For stage II decomposition, we recommend the TV- $\ell 1$ model an d the log TV- $\ell 1$ model to explain the piecewise smoothness and correlation within the residual S. In this section, we also demonstrate its effectiveness via simulation results. We use an image of chinese calligraphy as a spatially-correlated spares object, which has similar structure properties to the feature compensation part in the RTSD model. Parameter μ'is fixed as 1 for both TV - $\ell 1$ model and log-TV- ℓ l model in this section. The threshold *tol* is S2 = Sparse noise part temporal-spatially correlated information, e.g., background, is captured in **L**. For our applications discussed in this paper, e.g., video denoising and scratch detection, we choose RPCA to fulfill the Stage I decomposition from **M** to **L** and **S** due to its preferable robustness to outliers and background variations fixed as 10-7 in Algorithm 1 and Algorithm 2 (the same hereinafter); by this setting, both algorithms typically take 20-30 iterations to converge.

C. Application sketch Video denoising

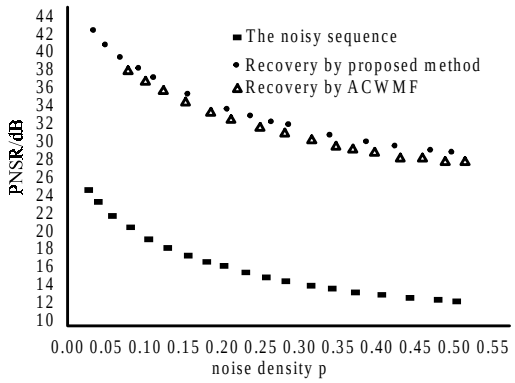
Since RTSD explicitly defines the **S**2 as sparse noise part, it is natural to find its applications in video denoising for sparse outliers (impulse noise). For impulse noise removal, we choose RPCA for Stage I decomposition and the TV-*l*1 model for Stage II decomposition. Many popular denoising methods, including those introduced in Section 1.1, emphasize the removal of i.i.d. Gaussian noise only. It should not be ignored that many video processing applications also involve long-tailed noise processes [36], resulting often from faulty sensors or transmission errors and thereby introducing sparse outliers in the gray values of the image, e.g., impulse noise. Removing impulse noise is quite different from removing Gaussian noise as the pixels damaged by impulse noise contain no original information. As widely recognized, impulse noise includes two main types: salt-and-pepper noise and random-valued impulse noise. Saltand-pepper noise only takes two extreme values (either 0 or 255 in 8-bit image) and is easy to detect and remove. In this section, we work on removing the more challenging randomvalued noise in our experiments, which is characterized by replacing a certain portion (denoted by *p*) of the original pixel values in the image with intensity values drawn from a uniform distribution between range [*dmin*, *dmax*] (*dmin*=0, *dmax*=255 in our experiments).

Classical denoising methods for impulse noise, e.g., [35], usually contain two stages, i.e., first detecting the locations of noisy pixels and then restore them. Their success relies on the accurate detection of noisy pixels, e.g., adaptive median filter (AMF) [36] for salt-and-pepper noise, as well as adaptive center-weighted median filter (ACWMF) [35] for detecting random-valued noise. In contrast, our method based on RTSD model does not require estimating the locations of noisy pixels before restoration as in two-stage methods. We test our method on video sequences with both simulated noise and real noise, and compare its denoising performance with the state-of-theart ACWMF method.

We first test our method on video data with simulated noise. 150 consecutive frames are chosen from the *"Paris"* sequence (352_288), and a portion *p* of randomly chosen pixels in the sequence are corrupted by random-valued noise. We reshape all frames to constitute the matrix **M**. Our final denoising result for the *i*th frame is obtained by adding **S**1(*i*) to **L**(*i*). The peak signal-to-noise ratio (PSNR) is used to measure the image recovery quality. It is worthy to discuss the parameter setting of our algorithm. In the first stage, we set λ'in the same way as what [23] suggests, i.e., 1?/ (352 _ 288). The μ'in the second stage should be adjusted according to the impulse noise density *p*. Based on our experience from repeated experiments, we recommend to set μ'according to a simple empirical formula: $\mu' = 2p + 0.8$, which can ensure an overall satisfactory performance when *p* is lower than 0.45. Experimental results presented in Fig. 3 and 4 demonstrate that applying our model in removing impulse noise outperforms ACWMF, in terms of both PSNR values and visual quality. In Fig. 3, we can view that ACWMF is likely to miss real noisy pixels and false-hit some noise-free pixels, which degrade the recovered frame visually in (h). On the

other hand, our method simultaneously identifies outliers and recovers damaged pixels, and produces pleasant visual results as shown in (g). Figure. 4 shows that under different noise densities, the recovery PSNR values of our method achieve a rise of about 20 dB to the noisy sequence, and are consistently higher than those of adopting ACWMF. Especially, when noise density is relatively high (e.g., $p >$ 0.3), the performance gap between our method and ACWMF turns even more significant (up to 2 dB). What is more attractive, our model does not require any assumption about statistical properties of impulse noise, except a rough estimation of noise sparsity p for setting the value of μ'.Actually, as verified in experiments, the denoising performance is to-some-extent robust to the choice of μ'.Even μ'deviates 10% away from its recommended values, the experimental results show that the PSNR decreases are generally less than 0.2 dB and the visual quality remains nearly unaffected.

To further demonstrate the denoising performance based on our RTSD model, we test our method on a 120-frame grayscale sequence (720 _ 540), which is collected from an aged video tape corrupted by impulse noise. Although the parameter μ'is empirically adaptive to p, which is unknown in practical situations, the probable estimation deviations do not obviously influence the denoising results. Therefore, we may first give a rough estimation of noise sparsity, which can be fulfilled by a plenty of traditional impulse detection methods, such as decision-based median filter [38] and rankordered mean (ROM) filter [39] (note that we do not care about whether each detection itself is accurate or not; only the estimation of noise sparsity p is enough). In this case, p is approximately 31.4%, thus we set μ'as 1.428 accordingly. We also use ACWMF to remove noise directly for comparison. Since the ground truth is unknown, we compare the two result visually (1st frame) in Figure. 5, which shows that our method performs significantly better in completely removing noise (e.g., on the tree leaf) and preserving structural details (e.g., on the animal).



Average PSNR performance comparison on the *"Paris"* sequence. It can be seen that under different noise densities, the recovery PSNR values of our method achieve a rise of about 20 dB to the noisy sequence, and are consistently higher than those of adopting ACWMF. Especially when noise density become relatively high (e.g. $p >$ 0.3), our method can even gain nearly 2 dB PSNR advantage over ACWMF.

Video denoising for the *"Paris"* sequence (with 20% impulse noise added) based on RTSD model. By the two stage decomposition, we get the decomposition results **L**(1), **S**1(1) and **S**2(1) corresponding to ~**M** (1), displayed in (c), (e) and (f), respectively. Our denoising result in (g) is obtained by adding **S**1(1) to **L**(1) (PSNR=34.28 dB). We also present the denoising result of the same frame by ACWMF in (h) for visual comparison (PSNR=33.62 dB).

CONCLUSION

RTSD is a model for temporal spatial decomposition and it presents how to obtain three parts from a video sequences step by step, provides efficient strategies to solve each stage of the model.

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Three Element Beamforming Algorithm

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ABSTRACT

The beam forming algorithm simulated in this project is motivated by analyzing low-cost radar system that provides wide spatial coverage and very rapid targ detection as well as tracking. Desigining towards these goals, a reasonable a... mostly generic receiver would employ a three-antenna receiver. Because the minimum number of sensing elements needed to determine two dimensional angles is three the system cost has been mostly minimized.

In this project 1 consider the problem of using our low cost system to detect and estimate the direction of arrival (DOA) of a desired signal in the presence of a dominant interference signal.

Unlike most direction of arrival (DOA) estimation algorithms, the proposed algorithm does not use grid search. Instead the estimates result from a closed-form solution, a great advantage in time-sensitive applications. Additionally, we carry out numerical simulations and results will be analyzed to demonstrate that our algorithm is capable of achieving more reliable DOA estimates than those found with the well-known multiple signal classification algorithm. Finally, a complete radar signal processing example will be presented.

MATLAB/GNU OCTAVE simulation tool will be used for simulation. The simulation results, applications, merits and demerits of proposed approach will be analyzed and will be documented.

Key words

three antenna receiver, direction of arrival

I. INTRODUCTION

A conventional technique of processing temporal sensor array measurements for signal estimation ,interference suppression, or source direction and spectrum estimation is beam forming [1-3].It has been exploited in numerous applications (e.g., radar, sonar, wireless communications, speech processing, medical imaging, radio astronomy).

The beam forming algorithm presented in this paper is motivated by analyzing low –cost radar system that provides wide spatial coverage and very rapid target detection as well as tracking. Designing towards these goals, reasonable and mostly generic receiver would employ a three antenna receiver. because the minimum number of sensing elements needed to determine two dimensional angles is three, the system cost has been mostly minimised..we now consider the problem of using our low cost system to detect and estimate the direction of arrival of a desired signal in the presence of dominant interfering signal.

The rest of the paper is organized as follows. In section 1,first,we give a full description of our algorithm ,starting with the system model and continuing with a tabular list of algorithm steps .Next we proceed with the system model and continuing with a tabular list of algorithm steps .Next ,we proceed with a detailed description on our methodology for interference cancellation ,target detection, and phase angle estimation. Afterwards, we analytically identify the spatial scenarios of a jammer and target in which the proposed technique will reliably estimate a target's DOA. Next, in section 3 the stastical performance of the algorithm is explained through a collection of simulations..Finally; section 5 contains the conclusions of this work.

II. SYSTEM MODEL

Three antennas in an arbitrary geometry make up our receiver structure. The received signal at the *i*th element at time n,is denoted by $x_i(n)$and is formed from the

coherent condition of the target signal $t_i(n)$,the jammer signal $u_i(n)$,and the noice $v_i(n)$.Therefore

$$x_i(n) = t_i(n) + u_i(n) + v_i(n) \qquad i = 1,2,3.....(1)$$

Assuming point sources and equal gains for the three receivers, the target and interfering signal at each sensor will be phased replicas [10].We also assume sensor will be phased replicas [10].We also assume narrow band signals, which means that relative phases of the received signal s will be constant across the entire band. the target signals are modelled as

$$t_2(n) = t_1(n)e^{j\theta}$$
$$t_3(n) = t_1(n)e^{j\delta} \qquad .....(2)$$

Where

$$t_1(n) = \alpha(n)e^{j\phi(n)} \qquad .....(3)$$

And the interfering signals are

$$u_2(n) = u_1(n)e^{j\in}$$
$$u_3(n) = u_1(n)e^{j\eta} \qquad .....(4)$$

Where

$$u_1(n) = \beta(n)e^{j\lambda(n)} \qquad .....(5)$$

The variables $\alpha(n)$and $\phi(n)$respectively denote the amplitude and the time varying phase of the target at antenna 1,while θ and δ denote the relative phase angles at antenna 2 and 3.In a similar manner ,the parameters $\beta(n),\lambda(n),\in$, ,and η denote the amplitude ,time varying phase ,and electrical phase angles of the jamming signal .The noise , $V_i(n)$is a white zero –mean complex random variable with variance σ^2 and is uncorrelated with $V_m(n)$for $i \neq m$ All greek letter variables represent real numbers.

We now give an overview of our algorithm which does not fit either of the paradigms introduced above, i.e. we do not scan a narrow beam nor do we use a parametric method to estimate the steering vectors of all present source signals. Throughout the rest of this paper, we refer to the desired signal as the target signal because this approach has been motivated from the signal processing needs of a radar system. we have also choosen to use a noise jammer for the interference source because of the ease at which one can be simulated, but application need not be limited to this case. the algorithm steps are enumerated in table I.Like [11] instead of using beam forming is used to null a jamming signal. Nulling the jammer enables a reduced –complexity mathematical technique for estimating target signal parameters. Unlike [11], we employ phase interferometery and require one less receiver channel. Adapting a beam based solely on information about an processing techniques that attempt to reduce computational complexity.

***Table1** : Algorithm overview*

Step1 : Find beam forming weights that minimize the jammer's power.

Step2 : Apply threshold detection to the Beamformer outputs of each range - Doppler bin of interest.

Step2a: If a target is detected,record its range and Doppler and proceed to step 3.

Step2b: If no target is detected, start over with the next coherent processing interval.

Step3 : Estimate relative phase information for each detected target.

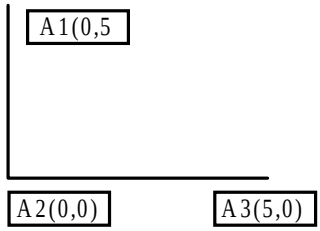
Step4 : Calculate DOAs from the phase information.

III. METHODOLOGY description-steps

I. Interference Cancellation

If a weighted sum of the received signals is formed, it is possible to choose non-zero, equal magnitude weights that completely cancel, or null the jammer signals. The importance of the weights being non-zero is obvious because we still desire to detect the target.

A L shaped is assumed with 3 antennas located at (0,5) ,(0,0) and (5,0) . A jammer signal is assumed to be located to predefined coordinates. The jammer signal is a cosine wave with random noise added to it. The goal is to nullify the effect of the three antennas due to the jammer signal. We calculate each of the antenna's net output due to the jammer signal by taking relative delays (time taken for the signal to reach the antenna) into consideration. The phase weights of each of the 3 antennas are calculated using the below formulas



Antennas(1,2) = X1 + X2 * e^(jwt)

Antennas(1,3) = X1 + X3 * e^(jwt)

The phase weights are calculated by varying the value of pi from -180 to 180 in steps of 0.0001.We find where the minimum value value occurs and consider the pi value to be the corresponding phase weight value. After obtaining the phase weight values, we multiply the respective phase weight with the antenna output the compare the results.

II. Target Detection and Range estimation

We assume the target coordinates and calculate the Radar signal for 3 pulses. We then observe the output when the radar emits the signal, how it is reflected from the receiver and how it is received back by the transmitter. The total antennas output will be the sum of the radar signal due to target and the jammer signal.

A threshold value is computed based on the assumed noise power. The complete antenna output is compared with this threshold value. If a match is found, the corresponding index is noted and the round trip time and the range of the target are both calculated. If no match is found the entire process is repeated with another set of radar pulse signals.

III. Angle of arrival (AOA)

The Angle of arrival is calculated building the look up table for sample delays between antenna outputs to DOA of signal. The angles are measured considering the line joining antenna 2 and 3 as initial line where the location of antenna 2 is the origin. All angles are measured in anti clock wise direction. For example if the target is on the line joing the 1 and 2 antennas then it will be reported as 90 degrees.

We first calculate maximum delays corresponding to Antenna pairs(1,2) and (2,3).Taking a loop from min to max value we calculate all the angles possible to the antenna pairs (1,2) and (2,3) by using the below formulae

Theta(1,2,1) = (180/π) * sind(dd12/d12)

dd12 : Additional distance travelled by the signal

d12 : Distance between Antennas 1 and 2

Theta(1,2,2) = - Theta(1,2,1)

Theta(2,3,1) = (180/π) * cosd(dd23/d23)

dd23: Additional distance travelled by the signal

d23 : Distance between Antennas 1 and 2

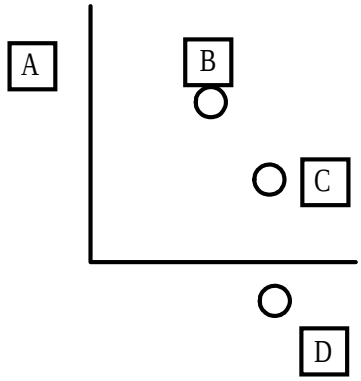
Theta(2,3,2) = - Theta(2,3,1)

After building the look up table we now calculate cross correlation between Antenna 1 and 2 outputs , Antenna 2 and 3 outputs. The maximum peak from the cross correlation outputs is found for the 2 antenna pairs.

Based on the maximum peak index the corresponding angles from the look up table are extracted for the Antenna pairs (1,2) and (2,3).Therefore 4 angles are obtained A and B for the first antenna pair, C and D for the second antenna pair. The angle of arrival is then found by taking the differences of the angles (A,C) , (A,D) , (B,C) and (B,D).

Wherever the least difference is obtained, angle of arrival is found by averaging the 2 angles where the minimum difference was obtained.

For Ex:



Angles due to Antenna pair (1,2) is A,B

Angles due to Antenna pair (2,3) is C,D

Taking all the differences, minimum difference is obtained from B and C.

Therefore angle of arrival = (B+C)/2.

IV. SIMULATION RESULTS:

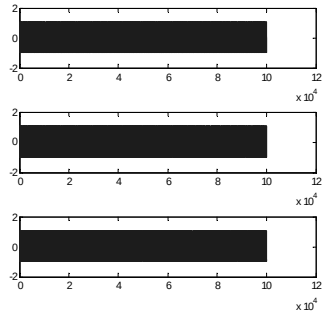


Fig.1 : *Data generation*

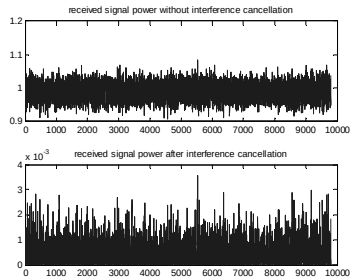


Fig.2 : *Interference cancellation*

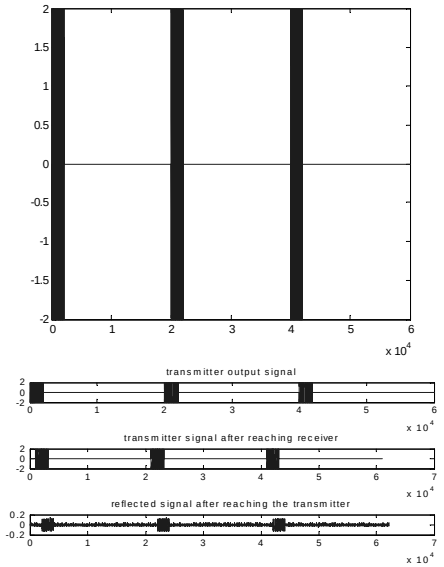


Fig.3 *: Radar signal generation*

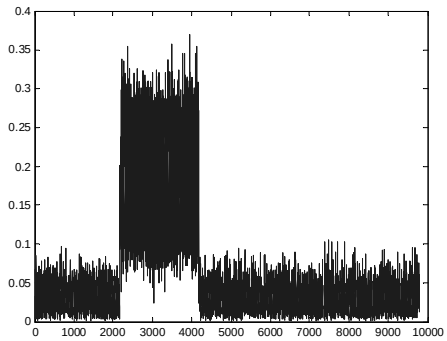


Fig.4 *: phase angle estimation*

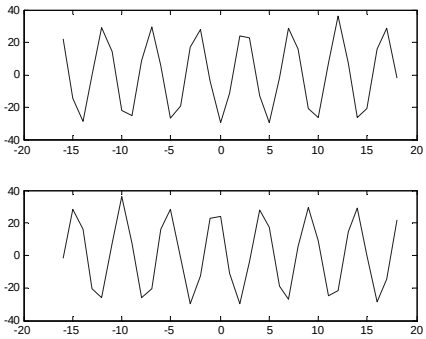


Fig.4 *: obtaining angle of arrival of desired signal*

V. CONCLUSION

While in the presence of a dominant interference source, our proposed algorithm yields unbiased target DOA estimates from a low-cost, three-element receiver. Unlike most DOA estimation methods, our estimates are found from closed-form expressions. In contrast to MUSIC, our algorithm performs well even when the number of target-containing snapshots available is small. This property makes it attractive for use in post-Doppler processing where it is common for a target signal to straddle only a few range-Doppler bins. Te DOAs of multiple targets can be estimated from one CPI as long as those target signals are resolvable in range or Doppler.

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Minimizing Leakage Power Wastage By Using Conditional Pulse Enhancement Scheme

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ABSTRACT

In this paper, a low-power pulse-triggered flip-flop (FF) designed and a simple two-transistor AND gate is designed to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 50-nm technology reveal that the proposed design features the best power-delay-product performance in several FF designs under comparison. Its maximum power saving against rival designs is up to 18.2% and the average leakage power consumption is also reduced by a factor of 1.52.

Keywords

Flip-flop, low power, pulse-triggered, pulse enhancement.

1. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a days often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–40% of the total system power [1].Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network [4].Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the Pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated.

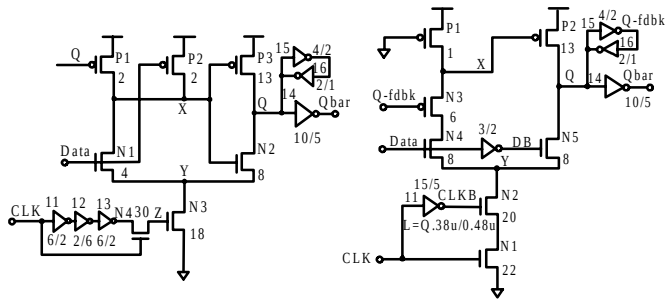

Figure. 1 : *Conventional pulse-triggered FF designs (a) MHLLF (b) SCCER*

In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives rise to competitive power and power–delay–product performances against other P-FF designs.

II. IMPLICIT-TYPE P-FF DESIGN WITH PULSECONTROL SCHEME

A. Conventional Implicit-Type P-FF Designs

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters. Two practical problems exist in this design. First, during the rising edge, PMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

Figure. 1(b) shows an improved P-FF design, named MHLLF, by employing a static latch structure presented. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistorP1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero. This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during “0” to “1”transitions because node x is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input Data both equal to “1”. Extra DC power emerges if node X is drifted from an intact“1”. Figure. 1(a)) is replaced by a weak pull up transistor P1 in conjunction. The discharge path contains MOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is “1” and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistorP1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

B. Proposed P-FF Design

The proposed design, as shown in Figure. 2, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of NMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is “1.” Refer to Figure. 2, the upper part latch design is similar to the one employed in SCCER design .As opposed to the transistor stacking design in Figure. 1(a) transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to “0” (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two NMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

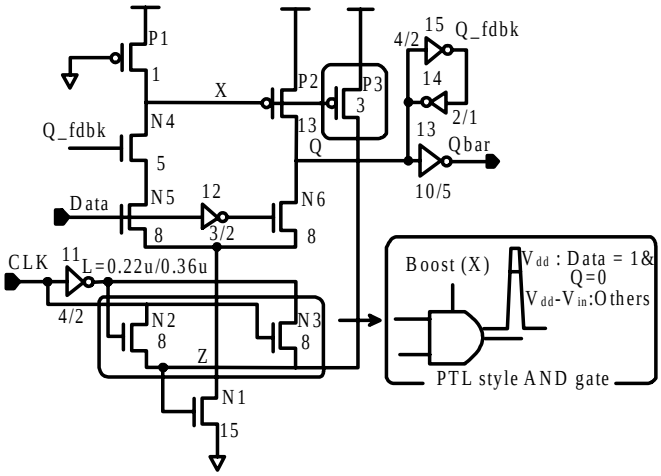

Figure.2 : *Schematic Diagram of the proposed P-FF design with pulse enhancement scheme.*

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time. It steps in when node X is discharged to VTP below the VDD. This provides additional boost to node X (from VDD-VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor N1.After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1.

III. SIMULATION RESULTS

To demonstrate the superiority of the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the two P-FF designs shown in Figure. 1 (MHLLF, SCCER), The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0 V.

P-FF	MHLFF	SCCER	PROPOSED
Numberof transitors/Layout Area(m^2)	19/93.02	17/80.07	19/79.2
Setup time(ps)	8.3	-58.1	-39.7
Hold time(ps)	82.2	59.3	85.1
Min data to Q Delay(ps)	177.1	112.9	107.2
Clock tree power W	7.82	12.58	8.03
Averagepower (100%Activity) W	35.96	36.27	31.11
Averagepower (50%Activity) W	27.61	28.46	22.65

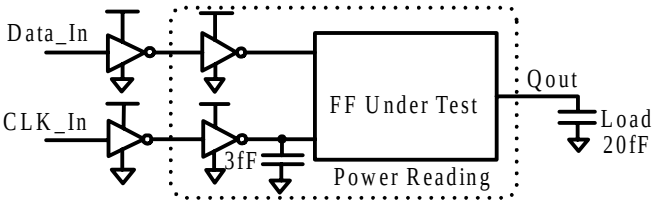

Fig 3 : *Simulation setup model.*

In general, the MHLLF design has the worst PDP_{DQ} performance due to the drawback of its latch structure. Figure. 6(a) shows the best PDP_{DQ} performance of each design under different data switching activities. The proposed design takes the lead in all types of data switching activity. The SCCER and the MHLFF designs almost tie in the second place. Figure. 6(b) shows the PDP_{DQ} performance of these designs at different process corners under the condition of 50% data switching activity. The performance edge of the proposed design is maintained as well. Notably, the MHLLF design has the worst PDP_{DQ} performance especially at the SS process corner due to a large D-to-Q delay and the poor driving capability of its pulse generation circuit. Table I also summarizes some important performance indexes of these P-FF designs. These include transistor count, layout area, setup time, hold time, min D-to-Q delay, optimal PDP, and the clock tree power.

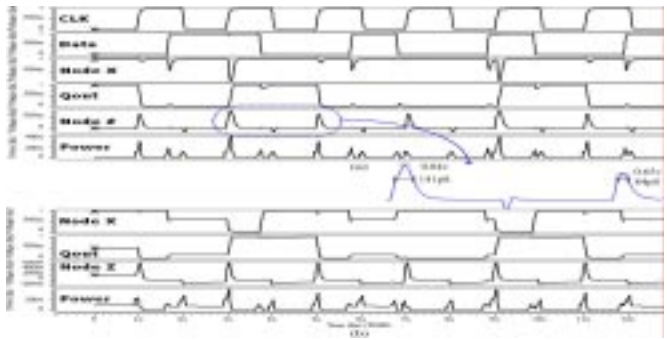

Figure.4 : *Simulation waveforms of (a) proposed and (b) MHLLF designs.*

Feature Comparison Of Various P-Ff Designs

Although the transistor count of the proposed design is not the lowest one, its actual layout area is the smaller than all but the TGFF design. The MHLLF design exhibits the largest layout area because of an oversized pulse generation circuit. Following the measurement methods in [6], curves of D-to-Q delay versus setup time and C-to-Q delay versus hold time are simulated first. Setup time is defined as the point in the curve where D-to-Q delay is the minimum. Hold time is measured at the point where the slope of the curve equals -1.

The proposed design features the shortest minimum D-to-Q delay. Its hold time is longer than other designs because the transistor (P3) for the pulse enhancement requires a prolonged availability of data input. The power drawn from the clock tree is calculated to evaluate the impact of FF loading on the clock jitter. Although the proposed FF design requires clock signal connected to the drain of transistor N2, the drawn current is not significant. Due to complementary switching behavior ofN2 and N3, there exists no signal path from the entry of the clock signal to either V_{DD} or GND.

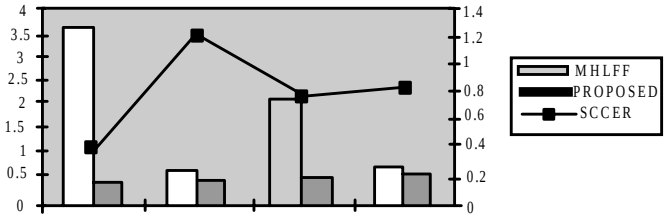

Figure. 6 : *Power–delay-product performances under (a) different data switching activities and (b) different processor corners at 50% data switching activity. (c) proposed flip in accordance with power dissipation*

Leakage Power Comparison In Standby Mody (μW)

FF/design/(CLK,Data)	(0,0)	(0,1)	(1,0)	(1,1)
MHLFF	3.656	0.666	2.161	0.763
SCCER	0.369	1.208	0.779	0.823
PROPOSED	0.444	0.481	0.582	0.624

Significantly better than other designs. The simulation results show that the clock tree power of the proposed design is close to those of the two leading designs (MHLFF and SCCER) and out performs of MHLLF, SCCER where clock signals connected to gates of the transistors only. The setup time is measured as the point where the minimum PDP value occurs. The setup times of these designs vary from -67 to +47 ps. Note that although the optimal setup time of the proposed design is -53.9 ps, its PDP value is lowest in all designs for any setup time greater than-60 ps. The D-to-Q delay and the hold time are calculated subject to the optimal setup time. The D-to-Q delay of the proposed design is second to the SCCER design only and out performs the conventional TGFF design by a margin of 44.7%. The hold time requirement seems to be slightly larger due to a negative setup time. This number reduces as the setup time moves toward a positive value. Table II gives the leakage power consumption comparison of these FF designs in a standby mode (clock signal is gated). For a fair comparison, we assume the output Q as “0” when input data is “1” to exclude the extra power consumption coming from the discharging of the internal node X. For different clock and input data combinations,the proposed design enjoys the minimum leakage power consumption, which is mainly attributed to the reduction in the transistor sizes along the discharging path.

Pulse Generation Against Process Variation ($P_{S/V}$)

Corner case	SS	SF	TT	FS	FF
Data =0	180.1/ 0.45	92.9/0.6 1	84.7/0.6 5	83.1/0.0 63	50.0/0. 77
Data =1	375/.5 1	167.5/ 0.86	141.3/ 0.84	145.4/ 0.87	87.7/1 .04

The SAFF design experiences the worst leakage power consumption when clock equals “0” because its two precharge PMOS transistors are always turned on. Compared to the conventional TGFF design, the average leakage power is reduced by a factor of 3.52. Finally, to show the robustness of the proposed design against the process variations, Table III compiles the changes in the width and the height of the generated discharge pulses under different process corners. Although significant fluctuations in pulse width and height are observed, the unique conditional pulse-enhancement scheme works well in all cases.

IV. CONCLUSION

In this paper, we design a novel low-power pulse-triggered FF design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, D-to-Q delay, and PDP. Coupled with these design merits is a longer hold-time requirement

inherent in pulse-triggered FF designs. However, hold-time violations are much easier to fix in circuit design compared with the failures in speed or power.

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Design of Light, Medium and Heavy Block Ciphers

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ABSTRACT

Block ciphers are extensively used in wireless communication systems. Block ciphers are designed to achieve certain security level. The security can be measured in terms of confusion and diffusion. The confusion is achieved using nonlinear operation such as substitution box and diffusion is achieved using linear operations such as addition, multiplication, bit or byte manipulations, etc. The linear and differential cryptanalysis indicates the level of confusion and avalanche values indicates the diffusion level. This paper provides the design details of light, medium and heavy block ciphers. The Advanced Encryption Standard (AES) is used for bench marking. Results are provided for achieving security level less than AES, equal to AES and greater than AES.

Key words

Wireless communication, AES, encryption, authentication, and security.

1.0 INTRODUCTION

Block ciphers are very important in wireless communication for achieving confidentiality and authentication. Block ciphers are used for realizing encryption, and hashing. The former is used for secure data communication, whereas the latter is used for authentication using message authentication code (MAC). Block ciphers are deployed in all wireless devices for authentication and encryption. GSM, CDMA, Wifi, WiMax, Bluetooth use block ciphers extensively for secure communication. The ideal implementation for secure wireless communication is to use encryption by block ciphers [1-2] and authentication by digital certificates [3].

Block ciphers are also used extensively in secure communication such as banking transactions, e-commerce, military applications, etc. Advanced Encryption Standard (AES) algorithm was standardized about 10 years back [4] and its security is questionable with the availability of improved computational speed and memory. Therefore, design of block cipher to withstand the attacks is a continuous process. Basically, the strength of block cipher lies with one round function of that cipher. Generally, a round function is designed using one nonlinear operation and three linear operations. These operations will help to withstand the various cryptanalysis attacks such as linear cryptanalysis, differential cryptanalysis, plain text attack, cipher text attack, side channel attack, etc.

In a round function, the nonlinear operation such as substitution box modifies the plain text and linear operations mixes these changes across the entire block so as to make it difficult to the attacker to trace the original plain text. Linear operations can be classified into two categories: 1) Linear operations which modify the plain text such as key addition, key multiplication, multiplication using MDS matrix, etc. 2) Linear operations which does not modify the plain text such as transposition of bits and bytes. The former helps to create diffusion and latter spreads the diffusion across the block. Both are required to achieve desired avalanche values.

Avalanche values of cipher text indicate the level of diffusion. A secure block cipher should exhibit a change of 50% of cipher text bits when any one bit of plain text is changed. Since one plain text bit affects more than 50% of cipher block values, it is known as avalanche effect. Any operation on plain text contributes to avalanche values. The operation can be either linear or nonlinear. However, a block cipher is designed using linear operations for achieving desired avalanche values.

Several linear operations are available for the design of block ciphers. For example, AES algorithm uses key addition, multiplication with MDS matrix and byte rotation. The former two operations create the new cipher values by changing the bit values of a block, whereas the third operation spreads out the changes.

The operation of block cipher, which is realized as per the specification, is known as electronic code book (ECB) mode. Another mode known as cipher block chaining (CBC) provides additional security beyond ECB due to additional operations.

In this paper, block cipher security level is analyzed. Since AES is the *de facto* standard algorithm, it is used for bench marking.

2.0 CLASSIFICATION OF BLOCK CIPHERS

For the purpose of analysis, block ciphers are classified as light, medium and heavy. The light block cipher is defined as a cipher, which requires the computational effort less than that of AES. A medium cipher requires effort equal to that of AES. A heavy block cipher requires effort more than the AES.

The assumption is that key search will be carried out using brute force method. Other short-cut methods such as linear cryptanalysis, differential cryptanalysis, any other attack will be ignored in this analysis. These are ignored mainly because they are applicable to a specific encryption algorithm. Since our objective is to estimate the effort for three types of block ciphers, the above assumptions are valid.

3.0 EFFORT ESTIMATION

In order to estimate the effort, the standard algorithms such as DES and AES are considered.

3.1 LIGHT-WEIGHT BLOCK CIPHER

The DES uses Feistel structure, permutations, key addition and substitution box. Since its key size is 56 bits, the required effort is much less than the AES. Similarly, AES with less than 10 rounds requires less effort compared to AES.

3.2 MEDIUM-WEIGHT BLOCK CIPHERS

AES and other five finalists of AES contest are medium-weight block ciphers [4].

3.3 HEAVY-WEIGHT BLOCK CIPHERS

Example of heavy-weight block cipher is Secure AES (SAES) [5-8], which is implemented with 8x8 MDS matrix and key multiplication in place key addition. These additional steps increase the effort beyond AES.

Similarly, AES in CBC mode is heavy-weight cipher [9].

4.0 RESULTS

The computation effort is normalized with that of AES. The results are shown in Table.

The table indicates the effort index for various algorithms. The effort index is the normalized value with respect to AES.

Table: *Comparison of various ciphers*

S.No.	Block cipher	Effort index
1	DES	$5.29X10^{-23}$
2	5-rounds AES	0.5
3	10-rounds AES	1.0
4	10-rounds SAES	4.0
5	AES in CBC mode	1.25
6	SEAS in CBC mode	5.0

The results indicate that block ciphers can be designed to operate as light, medium and heavy ciphers. The light-weight ciphers can be deployed in applications, where the computational speed is important and the amount of security required is less. The converse is true with respect to heavy-weight ciphers.

In future, the demand for the heavy-weight block cipher will arise due to availability of computational facilities. This will happen as long as Moore's law is effective. Designers should target for effort index of 10 for sustaining the attacks.

5.0 CONCLUSION

This paper has classified the block cipher into three types: light, medium and heavy. Suitable examples are provided for each type. The results are useful for the design and deployment of block ciphers in various applications.

Acknowledgement

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Image Recognition and processing Using Back Propagation Neural Network

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ABSTRACT

Abstract- The main objective of the present work is to provide a new approa for image recognition using Back Propagation Neural Networks. Initially original gray scale intensity image has been taken for transformation. The Input image has been added with Salt and Peeper noise. Adaptive median Filter has been applied on noisy image such that the noise can be removed and the output image would be considered as filtered Image. The new data matrix with new different set of values has been taken as original data matrix and saved in data bank.

Now for recognition, a new test image has been taken and the same steps as salt & pepper noise insertion, removal of noise using adaptive median filter as mentioned earlier have been applied to get a new test matrix. Now the average error of the second image with respect to original image has been calculated based on the both generated matrices an effort has been made to use the back propagation neural network on test data matrix with reference to original data matrix thereby producing a new matrix of the second image (test image). The total average error has been calculated on generated data matrix produced after the application of Back Propagation neural networks on test data matrix to check whether proper identification can be made or not.

Index Terms

Artificial Neural Network, The Feed forward back propagation neural network Gray scale intensity Image, Salt and Pepper noise, Adaptive median filter.

I. INTRODUCTION

The main aim of image processing is to alter the visual impact such that the information content improves and as a result the said image is more suitable than original image. This technique helps in getting a better visibility of any portion or feature of interest of an image and suppressing the information in other portion or feature of that image. Image Recognition has been dedicated with finding the identity of an object being observed in the image from a set of known labels. Different Recognition techniques are available for use but the selection of an appropriate choice of such techniques depends mainly on a given task at hand and some other related parameters. Soft Computing is an emerging field built up of latest techniques like fuzzy logic, artificial neural networks, evolutionary computation and machine learning. Each soft computing technique can be applied to produce solutions to any problem that are too complex or noisy to tackle with conventional methods. Artificial Neural Network has been one of the recent development tools that are inspired from biological neural networks. The main advantage of this new powerful tool is to use its capacity to solve problems that are not very easy to be solved by traditional computing methods.

The traditional computers use step by step approach in solving a problem and each step should be well defined and computable. The computer cannot solve the problem if any step that the computer needs to follow is not known. So to solve a problem using a computer need all knowledge of how to solve the problem. But Artificial Neural Networks are new techniques that follow a different way from traditional computing methods to solve problems. Artificial Neural Networks may be considered as much more powerful because it can solve problems where how to solve have been not known exactly. Uses of artificial neural network have been spread to a wide range of domain like image recognition, fingerprint recognition and so on. Artificial Neural Networks have the capability to adapt to learn, generalize and organize data. Some of the known

structures of artificial neural network are perceptron, Adaline, Madaline, Kohonen, Back Propagation.

II. RELATED WORK

The appearance of digital computers [1] and the development of modern theories of learning and neural processing both occurred at about the same time, during the late 1940s. The study of artificial neural systems (ANS) [2] on computers remains an active field of biomedical research. Since that time, the digital computer has been used as a tool to model individual neurons as well as clusters of neurons, which are called neural networks. Traditional techniques from statistical pattern recognition were popular until the beginning of the 1990s.In the new era, 2000, Robert P.W. Duin, and Jianchang Mao [3] gave us a holistic summary and compared some well known methods in pattern recognition system. The review was mainly meant for statistical approaches. Artificial neural network (ANN) was discussed there as a part. As it is found that statistical methods are more or less suffer from unavailability of general mathematical methods for recognition of features. A new approach for feature extraction based on the calculation of Eigen values from a contour was proposed and found that using feed forward neural network satisfactory results were obtained [4]. Artificial neural networks have increasingly been used as an alternative to classic pattern classifiers and clustering techniques. In the field of medical image processing, Kenji Suzuki [5] compared pixel based and non pixel based ANNs to show that the former approach is much better when it comes to segmentation and feature calculation. The paper also concludes that Massive-Training ANNs (MTANNs) can be used to enhance images. In 1993 review article on image segmentation, Pal and Pal [6] predicted that neural networks would become widely applied in image processing. Segmentation, based on neural networks is found to show rich capabilities [7]. Another related work in the domain of medical image processing shows artificial neural network for image segmentation. The approach was conjugated with real time applications. A hybrid neural network was proposed [8]. When compared with Eigen face method this hybrid neural network shows that error rate found to be producing satisfactory results. A more real time approach in the direction of the advancement of artificial neural networks has show that, how the detection and quantification of persons can be done in cluttered beach scenes [9]. It shows neural-based classification system. An approach to perform neutral facial image recognition using Parallel Hopfield Neural Networks [10], shows encouraging results in recognition rate. A survey based on Hopfield neural networks was published in the year of 2007[11], where a broad Theoretical review of the concept was presented. Object recognition consists of locating the positions and possibly orientations and scales of instances of objects in an image. The purpose may also be to assign a class label to a detected object. Some other types of ANNs like feed-forward artificial neural network approaches can also be used for object recognition.

Feed-forward networks usually consist of three to four layers in which the neurons are logically arranged. The first and last layers are the input and output layers respectively and there are usually one or more hidden layers in between the other layers. Here information is only allowed to “travel” in one direction. This means that the output of one layer becomes the input of the next layer, and so forward. In order for this to occur, each layer is fully connected to next layer and each neuron is connected by a weight to a neuron in the next layer.

A flow diagram for Image Recognition and Processing using Back Propagation Neural Network has been furnished in Fig -1

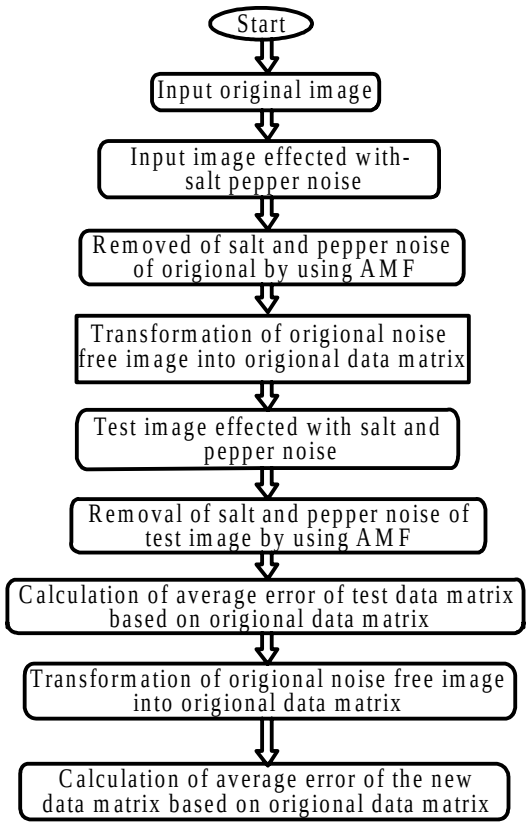

Fig -1 Flow Diagram

This paper aims to provide an alternative solution for object Recognition using Artificial Neural Network. Initially an original gray scale intensity image has been taken as a reference and it is saved as original data bank. For processing the method of transformation has been applied on the original image. Initially an original gray scale intensity image has been taken for transformation.

The Input image has been added with Salt and Peeper noise. Adaptive median Filter has been applied on noisy image such that the noise can be removed and the output image would be considered as filtered Image. The estimated Error and average error of the values stored in filtered image matrix as have been calculated with reference to the values stored in original data matrix for the purpose of checking of proper noise removal. Now each pixel data has been converted into binary number (8 bit) from decimal values. Then a set of four pixels has been taken together to form a new binary number with 32 bits. Thereafter the binary number has been converted into a decimal number. This process has been continued for whole image row wise such that a new data matrix with different set of values has been produced. This data matrix has been taken as original data matrix and saved in data bank for reference. Now for recognition, a new test image has been taken and the same steps as salt & pepper noise insertion, removal of noise using adaptive median filter as mentioned earlier have been applied to get a new test matrix use back propagation neural network on test data matrix with reference to original data matrix to produce a new matrix of the second image. The average error has been calculated on generated data matrix produced after applying Back propagation Neural Network on test data matrix. It has been observed that if the average error is less than that of the value obtained earlier then it has been concluded that the images are matching and therefore can be recognized.

III. IMPLEMENTATION

A. Processing of Original Image.

Step 1 : The initial optimal image has been taken as furnished in Fig -2 which has been considered as original image. For simplicity first 10X10 matrix elements of Original image are shown.

Table-1 : *Input Data Matrix*

158	159	159	158	155	153	153	154	150	158
155	156	156	155	152	151	151	152	151	160
153	154	155	154	152	150	151	152	153	162
154	156	156	156	154	153	154	155	156	164
153	155	156	156	155	154	155	157	159	166
151	153	154	154	154	154	155	157	163	166
152	153	155	156	155	155	157	159	166	165
154	156	158	159	158	159	160	162	167	164
156	158	159	158	160	163	166	167	167	164
161	161	160	160	161	163	165	165	164	162

Step 2 : The Input image has been added with Salt and Peeper noise.For simplicity first 10X10 matrix elements of Original image with Noise are shown.

Table -2 : *Input Matrix with Noise*

158	159	159	158	155	153	153	154	255	158
155	156	156	155	152	151	151	152	0	160
255	154	155	152	152	0	151	255	153	255
154	156	156	156	154	153	0	155	156	164
153	255	0	156	155	154	0	157	159	166
0	153	154	255	255	0	155	255	163	166
152	255	155	156	255	155	157	159	166	165
154	255	158	159	0	255	160	162	0	164
156	158	0	158	160	255	166	0	167	164
161	161	160	160	161	163	165	165	164	162

B. Processing of Noisy Image

Step 3 : Adaptive median Filter has been applied on noisy image such that the noise can be removed and the output image would be considered as filtered Image.

Step 4 : The original image after removal of noise has been transformed into data matrix containing pixel values which have been furnished in Table -3. For simplicity first 10X10 matrix elements are shown.

Table -3 : *Input Data Matrix after Noise Removal*

145	173	164	155	163	143	172	140	152	159
176	141	151	152	155	151	140	168	152	160
132	160	164	136	172	0	162	145	154	163
173	154	141	167	149	175	139	161	156	165
138	154	153	156	152	146	160	158	159	165
167	152	165	155	155	153	146	160	162	165
155	136	157	151	155	166	153	175	164	164
149	169	157	162	163	154	170	152	166	164
155	157	158	157	158	162	165	166	163	166
160	160	160	159	160	163	164	164	163	163

Step 5 : For easier calculation four pixels have been taken together. The four pixels have been taken row wise and converted into individual binary numbers.

Step 6 : The binary values of four pixels together side by side have been combined and formed as 32 bit binary number.

Step 7 : Now the 32 bit binary number has been converted into a decimal number.

Step 8 : The decimal number as generated in step 4 has been placed in original data matrix termed as ORMAT[][], which have been furnished in Table-4.

Table -4 : *Original Data Matrix ORMAT[][]*

2444076187	2744192028	2560599206	2846199930	1599955047
2962069400	2610400424	2560665254	2812448634	1583111782
2225120392	2885722769	2594416807	2778697081	1549426020
2912587175	2511309729	2628102566	2728168313	1566203236
2325387676	1559746206	2678433956	2711456630	1566269029
2811798939	2610533024	2728764833	2771456630	1583111782
2609421719	2611386799	2762252702	2711653493	1549426020
261079837	1661459366	2745607070	2661126013	1499029093
2694881439	2695013540	2745409178	2678497685	1482186084

Step 9 : The instructions furnished in step 6 to step 8 have been repeated for the total pixel value of the original image after noise removal as stored in Table -3. Therefore a matrix has been produced which has been stored in data matrix termed as ORMAT[][] as furnished in Table-4. It is to note that first 10X10 matrix elements are shown in Table-4 for easier presentation.

C. Processing of second Image (Test Image)

A new image has been taken which is considered as a Test image. Now it is necessary to check whether the said Image can be recognized or not. The test image has been Furnished in Fig-5. For simplicity first 10X10 matrix Elements of Test image (test data matrix) are shown as Furnished in Table-5. Test data Matrix.

161	160	160	159	158	158	158	158	155	155
155	155	155	154	154	154	154	154	153	153
152	152	153	153	153	153	153	153	152	153
154	155	156	156	156	156	156	155	153	153
155	156	157	157	156	155	154	153	148	147
154	154	154	154	152	149	146	145	137	135
154	154	153	152	148	144	140	138	129	126
156	156	155	152	148	143	139	136	126	123
156	155	153	151	148	144	139	134	130	121
160	158	156	155	153	150	146	143	136	127

Step 10 : Instructions as furnished in step 2 have been executed on test image to generate test data matrix with noise as furnished in Table -6. Test data Matrix with Noise

161	160	160	255	158	158	158	158	255	155
155	155	155	154	154	154	154	255	153	255
152	152	153	153	153	153	153	153	255	153
154	155	1556	156	156	156	156	155	153	153
155	156	157	157	156	155	0	153	148	147
154	154	154	154	152	149	146	145	137	255
154	154	255	152	0	149	146	145	137	255
0	156	155	153	0	143	139	136	126	0
156	155	255	151	148	144	139	134	130	121
160	158	255	153	150	150	146	143	136	127

Step 11 : Instructions as furnished in step 3 has been executed on test image with noise to generate test data matrix after noise removal as furnished in Table -7. Test data MATRIX After Noise Removal

160	161	160	158	155	154	154	156	149	159
155	156	156	154	152	151	152	153	151	159
152	153	154	153	152	151	152	154	151	156
152	154	156	156	154	154	154	156	151	151
152	154	156	156	154	153	153	154	153	149
151	153	154	153	150	148	146	146	152	146
151	152	153	151	147	143	140	139	141	134
152	158	156	152	145	147	138	136	128	122
157	158	156	151	145	141	137	134	130	120
162	161	158	154	150	148	145	143	137	127

Step 12 : Procedures as mentioned from step 4 to step 8 have been executed on test image after noise removal to generate the decimal number which has been placed in test data matrix TESTMAT[][], which have been furnished in Table -8.

2694946974	2610600604	15102268328	2846133877	1566857841
1610732186	2560071833	2543821987	2762051193	1749640558
2560203417	2560071834	2543623579	2627506047	2039212775
2560369468	2593823388	2543293584	2442309546	2355928947
2560269468	2593757594	2576715398	2206433146	1903127414
2543426201	256319250	2559739773	2004054125	1636001889
2543360407	2475658379	2374401397	1869244777	1701341285
2560268952	2475526792	2155508591	1802070636	1751408137
2644417687	2441972102	2188931182	1784963943	16678530056
2728500980	2526318991	2306831729	1818583910	1918727780

D. Calculation of Average Error of test data matrix based on original data matrix.

Step 13 : The estimated Error and average error of the values stored in decimal matrix as furnished in Table- 9 have been calculated with reference to the values stored in original data matrix as stored in Table 4. The average error has been found as 29%. The Estimated errors have been furnished in Table -9.

0.102644422	0.048650314	0.019655898	2.32074E-05	0.020686335
0.11861208	0.019280027	0.006577692	0.017919417	0.105190788
0.150590964	0.112849002	0.019577898	0.054410765	0.316173053
0.120963832	0.032856823	0.03270043	0.104783772	0.504229396
0.101007584	0.013287016	0.037976877	0.186216002	0.215070578
0.095445209	0.032259226	0.061941967	0.260893904	0.033408953
0.025316457	0.051975609	0.140411232	0.310662376	0.098046156
0.019653278	0.098110402	0.229020787	0.339537127	0.142781908
0.012877077	0.02468764	0.202751477	0.329244863	0.112622206
0.012475299	0.062595065	0.159749393	0.321043315	0.294525566

Step 14 : Since the average error is less than 45%, necessary steps regarding the processing of test image has been made using the technique of back propagation neural network for the purpose of recognition.

E. Processing of Image towards recognition using back propagation Neural Network.

Step 15 : The feed forward back propagation neural network has been used on the test data matrix of the test image for training and testing with reference to the original data matrix of the original image. A new data matrix named NEWMAT[][] has been produced as a result which has been furnished in Table -10. It is to note that the number of

columns of the data matrix ORMAT[][] or TESTMAT[][] or NEWMAT[][] has been one fourth of the total number of columns in the Original Image data or Test Image data. So it takes considerably less time to complete the training and Testing using BPNN.

Table-10 Data Matrix NEWMAT[][] after BPNN application

34996695	34996695	34996695	34996695	34996695
412714663	133924677	41271463	41271463	41271463
19807497 36	19807497 36	19807497 36	19807497 86	19807497 36
20463885 71	20463885 71	20463885 71	20463885 71	20463885 71
19761671 79	19761671 79	19761671 79	19761671 79	19761671 79
20347589 41	20347589 41	20347589 41	20347589 41	20347589 41
2025488160	2025488160	2025488160	2025488160	2025488160
2010595645	2010595645	2010595645	2010595645	2010595645
2011606687	2011606687	2011606687	2011606687	2011606687
1967583086	1967583086	1967583086	1967583086	1967583086

Test image	Noisy test image	Trest image after noise removal
5	6	7
Fig5	Fig6	Fig7
Fig9	Fig10	Fig11

Step 16 : Each value of the data matrix NEWMAT[][] has been converted into 32 bit binary number.

Step 17 : Now the 32 bit binary number has been divided into four 8 bit binary numbers.

Step 18 : Each 8 bit binary value has been converted into decimal and each of them has been considered as pixel values for four consecutive pixels row wise.

Step 19 : The instructions furnished in step 16 to step 18 have been repeated for the total values of the data matrix NEWMAT[][]. As a result a new modified data Matrix named MODMAT[][] has been produced as furnished in Table -11. It is to note that first 10X10 pixels are stored in Table -11 for better presentation.

Table -11 Modified Data Matrix MODMAT[][]

164	131	170	161	149	152	157	165	170	168
16	176	129	152	166	54	156	163	164	161
0	159	160	161	144	166	162	167	165	159
165	141	158	173	139	160	160	164	160	153
154	162	155	160	163	160	163	166	162	154
163	157	160	162	166	166	162	170	150	156
161	156	160	161	164	163	168	159	149	152
160	157	161	159	160	158	160	152	170	182
163	162	164	157	153	150	161	154	155	156
167	167	166	152	144	142	149	164	153	152

F. Calculation of estimated Error and Average Error.

Step 20 : The estimated error and average error of the values as stored in Table -11 with reference to the values stored in Table -3 The image based on values as stored in Table-11 has been formed which has been furnished in Fig-8.

Step 21 : Other test images as furnished in figure-9 have been taken for processing and recognition.

IV. RESULTS

A number of original and Test images have been taken and processed. The results are furnished as in Table -12.

Table-12 Result

SI.No	Original Image	Noisy Original Image	Original Image after noise removal
1	2	3	4
1	Fig2	Fig3 T	Fig4
2	Fig2	Fig3	Fig4

Test image	Noisy test image	Trest image after noise removal
5	6	7
Fig5	Fig6	Fig7
Fig9	Fig10	Fig11

Average error w.r.t to original image after noise removal	Test image after training using BPNN	Remarks
8	9	10
29%	Fig8	Recognition possible
87%	-	Recognition not possible

Fig 2
Input Original image

Fig 3
Noisy Original image

Fig 4
Original image after noise removal

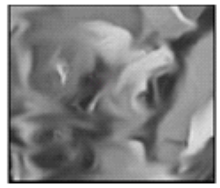

Fig 5
Test image

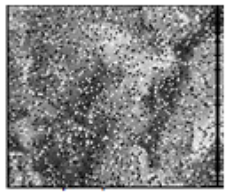

Fig 6
Noisy test image

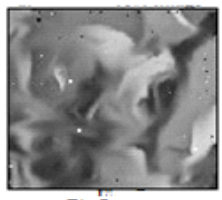

Fig 7
Test image after noise removal

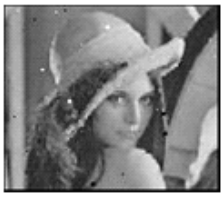

Fig 8
Image after training using BPNN

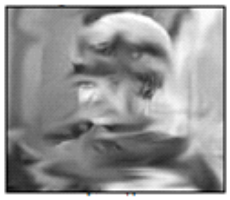

Fig 9
Test image

Fig 10
Noisy image

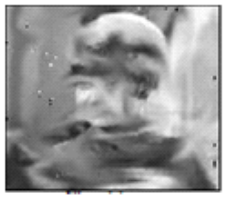

Fig 11
Test image after noise removal

V. CONCLUSIONS

It has been observed that if the average error is less than 45%, Back propagation neural network can be applied for training and testing for the purpose of recognition. Therefore the test image is recognized and matched successfully with original image. It has also been observed that, if the average error is greater than 45% then the image is recognized as a different image. In this paper salt and pepper noise has been inserted with an idea that all available images may contain certain noise which has to be removed for proper recognition. In this paper it has also been observed that it takes less time for training and testing using ANN as number of rows of the matrix used for training has one fourth number of columns compare to the original image.

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Call Loss Abatement and Data Stream Enrichment in Hierarchical Overlay Wireless Networks

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ABSTRACT

Oversubscription of Voice over internet protocol (VoIP) networks is prevent using Call Admission Control (CAC) .CAC is used in the call set-up phase a applies to real-time media traffic as opposed to data traffic. The basic idea is the blocked calls from fast-speed users are redirected to high-tier large Cells, and the slow speed users are redirected to low-tier cells. When calls are blocked due to cell capacity limits, blocked calls from fast-speed users are redirected to high-tier large cell, blocked calls from slow speed users are redirected to low-tier cells. This approach avoids frequent and unnecessary handoff between cells and reduces signaling overheads. A hierarchical overlay structure is an alternative solution that integrates existing and future heterogeneous wireless networks to ensure subscribers with better broadband mobile services. Traffic loss performance in such integrated heterogeneous networks is necessary for an operator's network planning and dimensioning. This paper investigates the computationally efficient loss performance modeling for multiservice in hierarchical heterogeneous wireless networks. An approximation model with guaranteed accuracy and low computational complexity is presented for the loss performance of multiservice traffic.

Key words - *Call Admission Control (CAC), Hierarchical overlay wireless network, Long Term Evaluation (LTE), Quality of Service (QOS), performance evaluation, Voice over internet protocol(VOIP)*

I. INTRODUCTION

Now a days with the extensive development and usage of mobile broadband services there is an urgent need for high speed and continuous Internet access. This can be achieved by integration of various hierarchical heterogeneous wireless networks viz., WiFi, Worldwide Interoperability for microwave Access (WiMAX), Third-Generation (3G), and Long-Term Evaluation (LTE) popularly known as 4G. A solution that integrates various wireless networks into a hierarchical overlay system based on a hierarchical cell structure has been considered [1]. This solution has been used for the deployment of femtocell networks in 3G, WiMAX, and LTE networks [2]–[4]. The advantage of this solution is that mobile users in the systems can switch between various wireless networks for more efficient use of network resources overheads. Additionally, frequent handoff can be incurred by mobile user's movement in those areas covered by small cells such a femtocells and leads to increased signaling overheads and operating costs. A solution to this problem is to take into account user mobility speed in call admission control (CAC) for mobility management as in cellular overlay networks In a WiMAX/femtocell overlay system presented in [2], mobile users can connect to the Internet via nearby femtocells, and the calls rejected by femtocell networks due to lack of radio access can overflow to overlaying WiMAX networks. Such kind of call overflow schemes has been used in cellular overlay networks for reducing call blocking probability to increased signaling overheads and operating costs. A solution to this problem is to take into account user mobility speed in call admission and improving bandwidth utilization [5], [6]. However, allowing call overflow between the overlay networks results in forced handoff and extra signaling. Additionally, frequent handoff can be incurred by mobile user's movement in those areas covered by small cells such as femto cells and leads control

(CAC) for mobility management as in cellular overlay networks [7]–[8]. When calls are blocked due to cell capacity limits, blocked calls from fast-speed users are redirected to high-tier large cells, e.g., macro cells; blocked calls from slow speed users are redirected to low-tier cells, e.g., microcells or femto cells. This approach assigns mobile users to appropriate cells so that frequent call handoff from fast-speed users in small cells can be avoided and signaling overheads reduced. In our current work, considering heterogeneous overlay networks, where the overflow traffic from different networks has different statistical moments (e.g., mean and variance), which are related to the service time distributions in these networks. In addition, the statistical moments of the overflow traffic offered to a new network are redefined according to the service time distribution in this new network. Basically the handoff schemes can be classified according to the way the new channel is set up and the method with which the call is handed off from the old base station to the new one. At call-level, there are two classes of handoff schemes, namely hard handoff and soft handoff. In hard handoff, the old radio link is broken before the new radio link is established and a mobile terminal communicates at most with one base station at a time. The mobile terminal changes the communication channel to the new base station with the possibility of a short interruption of the call in progress. If the old radio link is disconnected before the network completes the transfer, the call is forced to terminate. While in soft handoff, a mobile terminal may communicate with the network using multiple radio links through different base stations at the same time. The handoff process is initiated in the overlapping area between cells some short time before the actual handoff takes place. When the new channel is successfully assigned to the mobile terminal, the old channel is released. Thus, the handoff procedure is not sensitive to link transfer time. The second and third generation CDMA-based mobile communication systems fall in this category. Soft handoff decreases call dropping at the expense of additional overhead (two busy channels for a single call) and complexity (transmitting through two channels simultaneously). Two key issues in designing soft handoff schemes are the handoff initiation time and the size of the active set of base stations the mobile is communicating with simultaneously

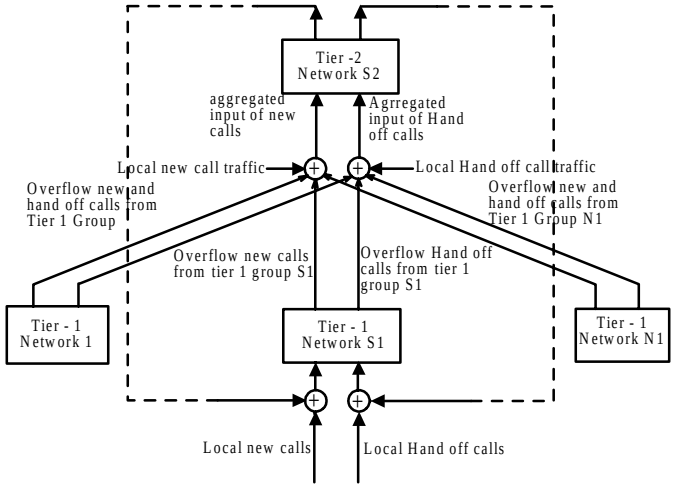

Fig. 1 : *traffic flows in a two-tier heterogeneous overlay system.*

I. HIERARCHICAL HETEROGENEOUS OVERLAY SYSTEM

Consider a two-tier overlay system with heterogeneous wireless networks distinguished from each other in capacity, signal coverage range, statistical characteristics of service time distribution, user mobility, volume, and traffic behavior. Here tire 1 has n number of networks these n number of networks come under one network of tier 2.The high tier networks are assumed to have greater signal coverage than those at the low tier; each high-tier network overlays several adjacent low-tier networks. The aforementioned speed-sensitive CAC scheme is used to manage the overflow traffic between the heterogeneous Overlay networks. Initially, if the new calls of fast-speed users in a low tier network are blocked due to capacity limits, the blocked new calls are overflowed to a high-tier network for possible service. If the blocked new calls are from slow-speed users in a high tier network, they are overflowed to a low-tier network. Similar control schemes are used to handle the handoff calls between the neighboring networks at the same tier. If fast-speed users in a low-tier network cannot be handed off to a neighboring network, their handoff calls are overflowed to the networks at the high tier. The failed handoff calls of slow-speed users in the high-tier networks are overflowed to the networks at the low tier. With this scheme, a call is finally dropped when there is no bandwidth available for it in the hierarchical system; call blocking and dropping probabilities can thus be improved. Additionally, using the bandwidth reservation scheme [10] to protect handoff calls. A portion of capacity in each tier network is reserved for handoff calls only; the remaining bandwidth is shared by all arriving calls. For simplicity, the bandwidth required by a class-*k* call, which is denoted d_k, is measured by the number of BUs.

II. PROPOSED LOSS PERFORMANCE MODEL

A. WLAN for VoIP: Voice capacity, admission control, QoS, and MAC

Voice over internet protocol (VoIP) is one of the fastest growing Internet applications. It is a viable alternative to the traditional telephony systems due to its high resource utilization and cost efficiency While, Wireless Local Area Networks (WLANs) have become a ubiquitous networking technology that has been deployed around the world. Driven by these two popular technologies, Voice over WLAN (Vo WLAN) has been emerging as an infrastructure to give low-cost wireless voice services. However, VoWLAN poses significant challenges since the performance characteristics of wireless networks are much worse than that of their wire line counterparts, and the IEEE 802.11-based WLAN was not originally designed to support delay-sensitive voice traffic. In this paper, providing a survey of recent advances in VoWLAN voice capacity analysis, call admission schemes, and medium access control (MAC) layer quality of service (QoS) enhancement mechanisms. MAC (Medium Access Control) protocol was designed for point-to-multipoint broadband wireless access applications. It addresses the need for very high bit rates, both uplink (to the BS) and downlink (from the BS).

B. WiMAX femtocells: a perspective on network architecture, capacity, and coverage

Femtocells are viewed as a promising option for mobile operators to improve coverage and provide high-data-rate services in a cost-effective manner. The idea is to overlay low-power and low-cost base station devices, Femto-APs, on the existing cellular network, where each Femto-AP provides high-speed wireless connection to subscribers within a small range. In particular, Femto-APs can be used to serve indoor users, resulting in a powerful solution for ubiquitous indoor and outdoor coverage, using a single access technology such as WiMAX. In this article considering a WiMAX network deploying both macro BSs and Femto-APs, where it is assumed that Femto-APs have wired backhaul such as cable or DSL and operate on the same frequency band as macro BSs. Simulation results show that significant areal capacity (throughput per unit area) gain can be achieved via intense spatial reuse of the wireless spectrum. In addition, Femto-APs improve indoor coverage, where the macro BS signal may be weak. Motivated by the gains in capacity and coverage offered by femtocells, review the state of the art of this "infant" technology, including use cases and network deployment scenarios, technical challenges that need to be addressed, and current standardization and industry activity.

C. On femto deployment architectures and macrocell offloading benefits in joint macro-femto deployments:

Macro and femtocells provides insights on possible deployment architectures for femtocells along with an analysis framework for quantifying macro offloading benefits in realistic network deployment scenarios by means of advanced performance analysis techniques. Such benefits include potential enhancement in quality of radio signals for users served by the macro network in joint macro-femto deployments. This in turn translates into potentially better data rates (throughput) for macrocell users and may offer the possibility of adding more users to the macro network while preserving the network configuration—resulting in direct capital expenditure savings. The approach taken in this article consists of creating a framework for quantifying macro offloading benefits in joint macro-femto deployments. A baseline configuration where all users (indoor and outdoor) are served by a traditional macro network (state-of-the-art macro only network) is considered first. The analysis is followed through joint macro-femto deployments, where femtocells serve indoor users. Through comparison of the baseline configuration and the joint macro-femto analysis, quantifying the benefits of the joint macro-femto deployment.

D. Hierarchical macrocell overlays for Micrcellular communication systems

A hierarchical overlaid scheme suitable for high-capacity microcellular communications systems is considered as a strategy to achieve high system performance and broad coverage. High-telegraphic areas are covered by microcells while overlaying macro cells cover low-teletraffic areas and provide overflow groups of channels for clusters of microcells. New calls and handoff calls enter at both the microcell and macrocell levels. Handoff calls are given priority access to channels at each level. The layout has inherent load-balancing capability, so spatial telegraphic variations are accommodated without the need for elaborate coordination of base stations (wireless gateways). An analytical model for telegraphic performance (including handoff) is developed. Theoretical performance characteristics that show carried traffic as well as blocking, handoff failure, and forced termination probabilities are derived. Effects of no uniform teletraffic demand and channel allocation strategies on system performance are discussed.

E. On the design of mobility management scheme for 802.16-based network environment

The characteristics of IEEE 802.16 and conclude that it is better to equip BS (base station) and SS (subscriber station) with Layer 3 functionality. Therefore, an 802.16 network can act as the backbone network of different subnets for better deployment. Based on the two IEEE Specifications, 802.16-2004 and 802.16e, we propose two kinds of paradigms of the 802.16 network technology for mobile networking. In the first paradigm, a novel concept called middle-domain mobility management in between macro- and micro-domain for 802.16-2004 is proposed. The management scheme of middle-domain is designed to accommodate different micro-mobility protocols in an 802.16-2004 network environment. Moreover, a mathematical analysis and simulation study are presented for performance evaluation. In the second paradigm, by comparing with traditional overlay networks (e.g. GPRS/WLAN), we have found that the characteristics for the 802.16e/802.11 overlay network are actually different from traditional overlay networks. To ensure more efficient vertical handoff, a novel protocol called speed-based vertical handoff scheme (SVH) is proposed. A Simulation study has demonstrated that SVH can achieve a better performance than its WLAN-first counterpart in terms of less signaling and fewer packet losses

III. MODULE DESCRIPTION

A. Deign of Heterogeneous wireless networks

Consider heterogeneous overlay networks, where the overflow traffic from different networks has different statistical moments (e.g., mean and variance), which are related to the service time distributions in these networks. In addition, the statistical moments of the overflow traffic offered to a new network are redefined according to the service time distribution in this new network.

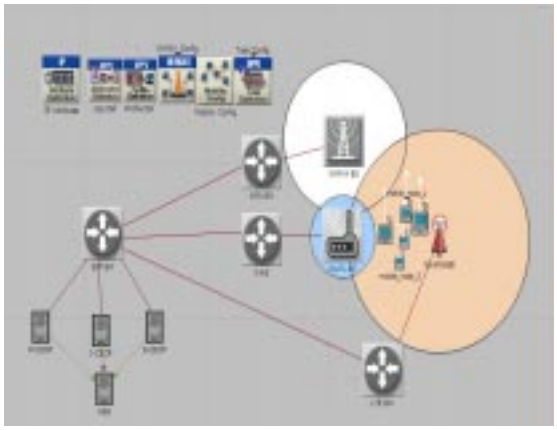

Fig 2: overlay of different heterogeneous networks

B. call admission control (CAC) scheme

With the speed-sensitive CAC scheme [9], bidirectional call overflows, both upward and downward, are supported in the hierarchical heterogeneous overlay systems. Blocked calls from fast-speed users are overflowed to the higher tier networks with larger coverage; blocked calls from slow-speed users are overflowed to the lower tier networks with smaller coverage. For conciseness, elaborating our model by assuming that only upward overflow traffic from fast-speed users exists. The same analysis method can be used for downward overflow traffic from slow-speed users.

C. Data traffic management

IEEE 802.21 module uses the make-before-break (MBB) algorithm for the seamless handover. In this algorithm mobile node connect with new network before terminating its previous network. By using the MBB algorithm mobile node will use both interfaces at the same time in order to perform a seamless handover. IEEE 802.21 add-on modules uses only signal strength and the interface type for the interface selection. The proposed and implemented algorithm uses the available bandwidth, coverage radius, user mobility and power of the battery along with RSS for the interface selection. Access of different networks causes the different level of the battery power consumption, due to difference in energy required for transmitting and receiving the packets.

The battery power consumption for the WiFi interface is more than the power that of WiBro (mobile WiMAX) interface. MN can be in normal mode or power saving mode. If the MN is in power saving mode there is no handover from WiMAX to Wi-Fi because of battery power consumption for WiFi is more than WiMAX interface and to avoid power loss during handover.

IV. PERFORMANCE EVALUATION

A. Handovers

A system or network performance is evaluated based on some parameters; here considering handover generally a handover or handoff refers to the process of transferring an ongoing call or data session from one channel connected to the core network to another. Performance is measured under the successful handovers a system can make without the termination of the call.

B. Packet drop

Generally a packet contains group of messages or information. An efficient network is one which gives the minimum packet drop, the less the packet drop the more will be the network performance. Here making a minimum packet drop service.

C. Time delay

The time gap between the sent message and received message is known as the time taken for message transmission. Delay in ideal case must be always minimum or zero. Network performance is also evaluated through time delay.

V. Simulation Results

In this section, showing and analyzing the simulation results of overall Packet delivery ratio, overall throughput, delay comparison, overall communication comparison, performance under different packet loss rates, call dropping probability, and also taking different nodes under different base stations

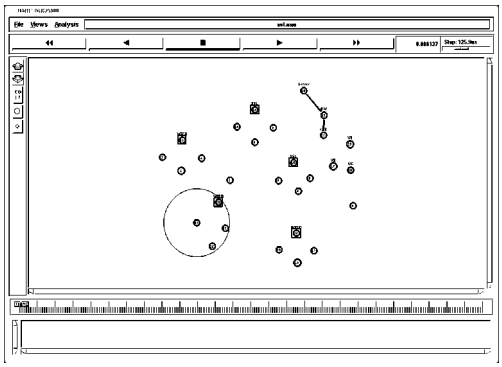

Fig 3 : *different nodes under different base stations*

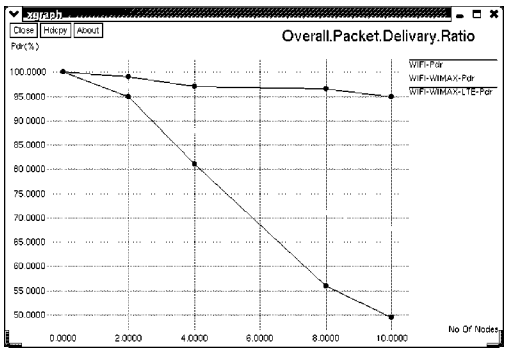

Fig 4 *: gives overall packet delivery ratio in . wifi-wimax-lte.*

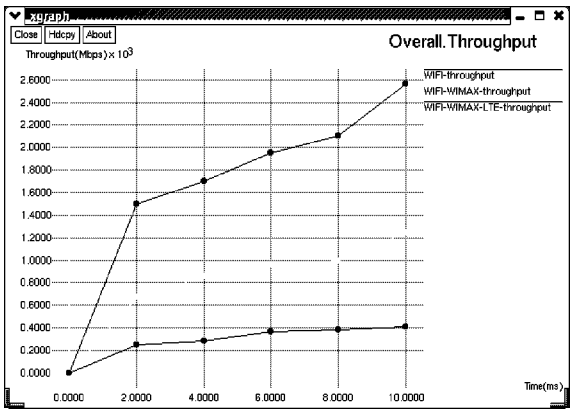

Fig 5 : *In this graph showing overall throughput for wifi, wifi-wimax, wifi-wimax-lte.*

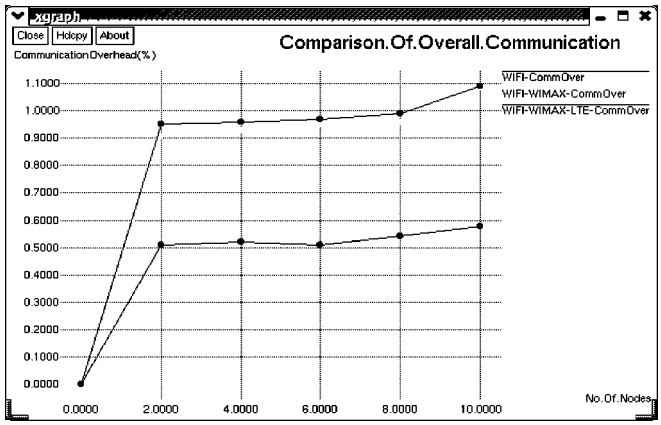

Fig 6 : *communication comparison between wifi, wifi-wimax, wifi-wimax-lte*

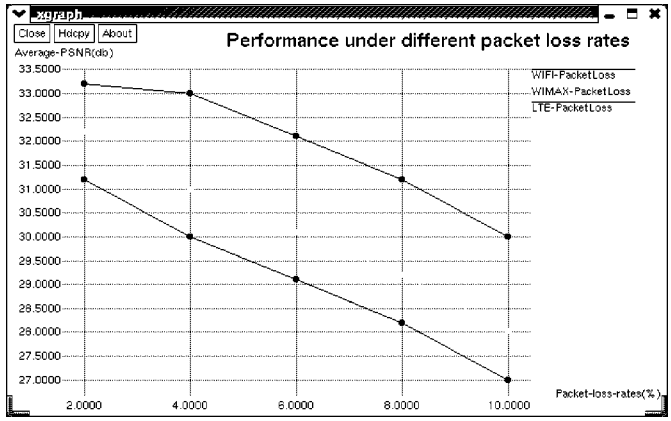

Fig 7 : *performance under different packet loss rates for wifi, wimax, lte.*

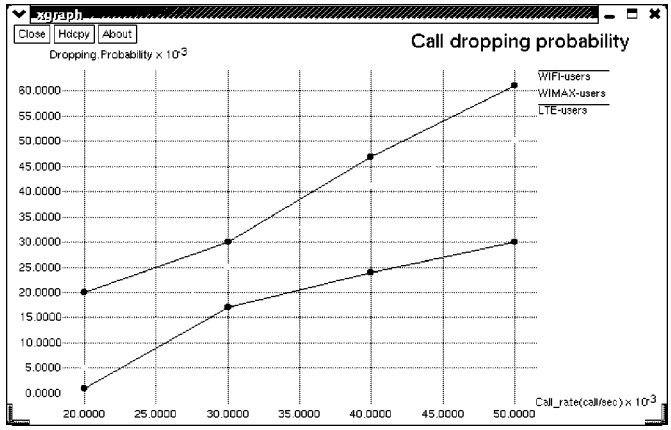

Fig 8 : *call dropping probability in wifi, wimax, lte.*

VI. Conclusion

Explaining graphically the overlay networks performance by calculating the overall throughput of the hierarchical networks (Wi-Fi-Wimax-LTE) and compared that the use of a speed-sensitive CAC scheme in hierarchical heterogeneous overlay networks helps improve the call-level loss performance.

As an extension to this project, we can still integrate future coming wireless networks which can further improve

the quality of service and provides better data streaming experience for the users with less delay and efficiency base individually. Proposed here a comprehensive loss model to obtain the numerical solution of multiservice loss performance in hierarchical heterogeneous overlay networks. By taking the effects of bandwidth reservation, user mobility, cell coverage, and varying service time distributions for cells at the same or different tiers into consideration. We have also demonstrated that the use of a speed-sensitive CAC scheme in hierarchical heterogeneous overlay networks helps improve the call-level loss performance.

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Improved ABICM Based on Expurgated Bound for Cellular Radio Orthogonal Multicarrier System

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ABSTRACT

Adaptive coded modulation is a powerful method for achieving a high spectral efficiency over fading channels. The cellular radio orthogonal multicarrier system improves the spectral efficiency. A long range fading prediction is very useful for maintaining reliability of channel state information. Adaptive modulation techniques are used to maintain the target bit error ratio. The unwanted noise predicted to the probability of error associated with transmission over discrete memory less channels. The proposed method in this paper improves performance of spectral efficiency for ABICM by combining both fading prediction and expurgated bound

Keywords

Adaptive Bit Interleaved Coded Modulation (ABICM), Channel State Information (CSI), Long Range Prediction (LRP), Trellis Coded Modulation (TCM), Orthogonal Multicarrier System, Bit Error Ratio (BER).

I. INTRODUCTION

Wireless communication industry necessitates the techniques which facilitates the efficient and improved communication which solves all the possible technical challenges to maintain the quality of wireless link .As the signal propagates through the mobile radio channels, it experiences random fluctuations in both time and frequency domain due to rapidly varying channel conditions. For mobile communication systems, where the channel is varying with respect to time it becomes essential to predict the information about channel state referred to as "channel state information(CSI)" for maintaining the efficiency of wireless link. The estimation about CSI is done due to the fact that there is always time difference between the time that the channel is measured and the time the corresponding transmission is made. Depending on the predicted channel condition the transmitter selects the appropriate modulation and transmission parameters. This process is known as "Adaptation". When the adaptation decision is made by the transmitter and the receiver needs to be informed about the selected transmission parameters and vice versa. This method is referred as CSI feedback. The steps required for maintaining reliability of CSI are: Prediction, Adaptation, and CSI feedback [1]. ABICM proposed in [2] is based on censored bound aided by fading prediction. This method improves the accuracy of BER when compared to the original ABICM method proposed in [3].The original ABICM method is based on Bhattacharya bound. The Bhattacharya bound is based on minimum distance of constellation and a nominal non-adaptive BICM scheme were employed to determine the constellation size and the transmission power. By using the original ABICM method the bit error rate deviates significantly than the actual bit error rate. Therefore, ABICM method based on censored bound is employed for mobile radio orthogonal multicarrier systems for its improved performance [4]. The ABICM also gives better spectral efficiency comparing to the methods that are proposed in last 20 years. The Adaptive Trellis Coded Modulation (ATCM) gives the better performance of spectral efficiency for reliable CSI but as the CSI becomes outdate the performance of ATCM

decays very sharply [5]. Thus, ATCM does not comprise a better performance for unreliable CSI.ATCM is also more sensitive to prediction errors than uncoded adaptive modulation (UAM) techniques. The UAM technique was investigated before the ATCM [6]. Hayes proposed the adaptation of transmission power when the channel quality varies but the drawback of this approach is it increases the peak power of interference to other users. To improve system capacity the trellis code was proposed on adaptive modulation. But this scheme achieves coding gain in the fading channel only when the CSI is accurate [7]. Zehavi recognized that reliability and code diversity of coded modulation (CM) over a Rayleigh fading channel can be improved by introducing bit wise interleaving at the encoder output and appropriate soft decision bit metric as an input to the Viterbi decoder. This technique is known as bit interleaved coded modulation (BICM).The interleaving is introduced to minimize the error probability. BICM is more robust to prediction errors than the trellis coded modulation (TCM).The time diversity of systems operating over fading channels can be improved by using BICM by providing an independent fading component for each channel bit out of the convolution encoder as oppose to each channel symbol [8]. Thus the adaptation of BICM systems is more effective than adaptation of TCM techniques for analyzing the performance of bit error rate (BER).The ABICM method is thus introduced to maintain the performance of bit error rate (BER).

The organization of the paper is as follows: Section II gives the adaptive modulation for orthogonal multicarrier system. Section III explains the ABICM with imperfect CSI. Section IV gives the graphical analysis for comparing different method for BER and spectral efficiency. Section V gives the Conclusion and future scope.

II. ADAPTIVE MODULATION FOR ORTHOGONAL MULTICARRIER SYSTEMS

A. System Model

The block diagram of the adaptive modulation for orthogonal multicarrier system under investigation is shown in Fig.1. Assume a frequency selective wide-sense stationary (WSS) Rayleigh fading channel. The received signal for the 1^{th} sub carrier l = 1,2, …L of the n^{th} orthogonal multicarrier system symbol is

$$Y(n,l) = H(n, l)X(n, l)+w(n, l) \quad .....(1)$$

Where H(n,l) and w(n, l) are the complex Gaussian channel response H(n,l)~CN(0,1) the transmitted signal, and the complex additive white Gaussian noise with variance N_o respectively. It is assumed the inter-symbol interference (ISI) is removed using an appropriate cyclic prefix. Without loss of generality, we set $X(n,1)=E_p$ for pilot symbols, where E_p is the pilot symbol energy.

To facilitate the LRP [9], pilot symbols are inserted in both frequency and time domains. Past pilot observations within a rectangular area that includes $2P_f+1$ pilot tones and P_t past pilot orthogonal multicarrier system symbols are employed to predict the current channel coefficient H(n, l) . In this letter, we assume that channel statistics are known and construct a linear minimum mean square error (MMSE) predictor of order $(2P_t+1)P_t[2]$. In practice, similar prediction accuracy can be achieved by the auto-regressive (AR) model based predictors that track fading channel variations [10]. The performance of this predictor can be improved at low and medium SNR by employing noise reduction [11].

However, we do not utilize noise reduction since we focus on robustness of adaptive coding methods to imperfect predictions. The channel coefficient H(n, l) and its linear MMSE prediction $H(n,l)$ are jointly Gaussian distributed [12]. The quality of prediction is usually measured by the prediction MMSE

$$\sigma^2 = E\left[\left|H(n,l) - H(n,l)\right|^2\right] \quad .....(2)$$

Suppose the maximum Doppler frequency of the channel is f_{dm}, and we need to predict τ second ahead of the most recently observed orthogonal multicarrier system symbol. Then the corresponding normalized spatial prediction range is $f_{dm}\tau$, which is usually expressed in the unit of carrier wavelength λ.

B. Adaptive Bit and Power Loading

At the transmitter, the information bits are encoded using a fixed-rate convolution encoder, followed by bit-interleaving. Due to frequency diversity in orthogonal multicarrier systems, this assumption is realistic even for short interleaving depth in time. After interleaving, the adaptive bit and power loading algorithm maps the coded bits into M-quadrate amplitude modulation (MQAM) symbols for all sub carriers. The constellation sizes and energies of these symbols are determined using the CSI fed back from the receiver. Without loss of generality, we consider the allocation for one orthogonal multicarrier symbol X(n, l).

Given predicted channel Coefficient $H(n,l), l \in [1,L]$, suppose the minimum average symbol energy required to transmit m_l coded bits/symbol while maintaining the target BER is $E_{H(n,l)}(m_l)$. Our objective is to maximize the spectral efficiency under the overall energy constraint E_T, i.e.,

$$\max\left\{\sum_{l=0}^{L} m_l\right\} \text{ subject to } \sum E_{H(n,l)}(m_l) \le E_T. \quad \text{.....(2)}$$

If $E_{H(n,l)}(m_l)$ is known, the discrete water filling algorithm based on the greedy principle achieves the optimal solution of (2) [11]. However, it is difficult to determine the function $E_{H(n,l)}(m_l)$ for given $H(n,l)$.

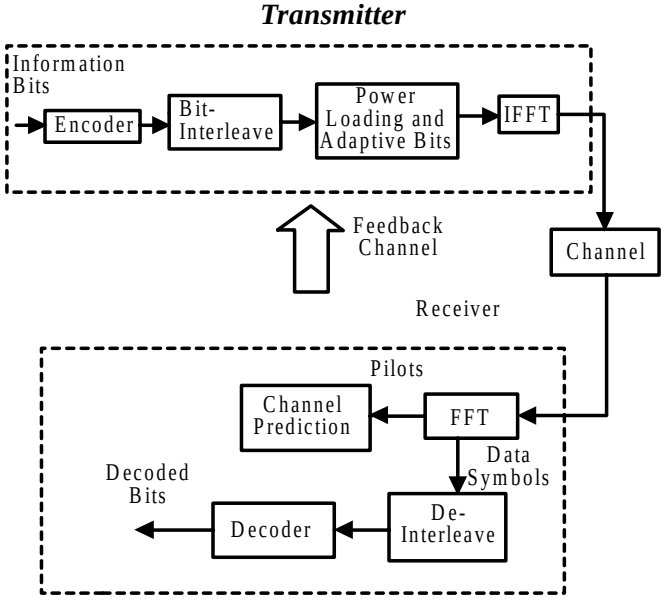

Fig. 1 : *Block Diagram of LRP-enabled Adaptive orthogonal multicarrier system with ABICM.*

This problem requires a tight analytical estimate of the average BER for each modulation level as a function of the predicted CSI. For thoroughly studied uncoded adaptive modulation [12] and ATCM, the function $E_{H(n,l)}(m_l)$ can be derived from the BER analysis of MQAM and trellis coded modulation (TCM) in AWGN channel[13]. However, for ABICM, previously proposed techniques do not provide accurate BER estimates as discussed earlier. In the following section we review the original ABICM method in and propose a novel technique based on the censored bound.

Where P_t is the target BER, W_1 (d) is the weight of error events at Hamming distance d, k_c is no. of bits input to the encoder.

III. ABICM WITH IMPERFECT CSI

A. Original ABICM Method

The original ABICM Method, which uses Bhattacharya Bound for single symbol error probability. The Bhattacharya bound of this error probability is

$$P\left[X \to X \middle| H(n,l)\right] \le \frac{1+K}{1+K+C}\exp\left(-\frac{KC}{1+K+C}\right) \quad \text{.....(3)}$$

Where, $K = |H(n,l)|^2/\sigma^2$, $C = d^2_{\min,m}(K+1)\sigma^2/(4N_0)$, $d_{\min,m}$ is the minimum Euclidean distance, $H(n,l)$ is predicted channel coefficient and N_0 is the noise variance. Both X and $\hat{X}$ are selected from constellation X_m. For, relating this bound to the target bit error rate a non-adaptive BICM scheme called as nominal scheme, which uses fixed MQAM modulation is employed [14]. The energy required to use the constellation X_{ml} for 1^{th} sub carrier to maintain target bit error rate is equation 3. This scheme faces the potential problems. 1) In equation 1, the single symbol error probability is considered while the performance is measured by the bit error rate. 2) The Bhattacharya bound in equation 1, is inaccurate. Therefore the bit error rate of this method deviates significantly from the target bit error rate as in equation 1.

$$E_{H(n,l)}(m_1) = \arg\min_{E_{ml}}\left\{\frac{1+K}{1+K+C}\exp\left(-\frac{KC}{1+K+C}\right) \le D_0\right\} \quad \text{.....(4)}$$

B. ABICM Based on censored bound

For maintaining the bit error rate to the target BER the ABICM based on censored bound is introduced by Tao Jia. The censored bound is also introduced for non-adaptive BICM. But, it is for reliable channel state information. The censored bound employed on ABICM method is for predicted channel state information. The censored bound is the pair-wise error probability (PEP) with the knowledge of H and X_m. The average symbol energy that satisfies the target bit error rate is,[eq.(5) in 1.

$$E_H(m) =$$

$$\arg\min_{E_m}\left\{\frac{1}{k_c}\sum_{d=d_{free}}^{\infty} W_I(d)\, f_{ex}(d,\mu,\chi_m, H \le P_t\right\} \quad \text{.....(5)}$$

IV. NUMERICAL RESULTS

A. Simulation Setup

We consider an orthogonal multicarrier system that has 120 sub carriers and the sub carrier spacing of 10.94KHz. The total bandwidth of this system is about 1.3MHz. We assume that the carrier frequency is2.5GHz, which is typical for the Mobile WiMAX deployment. The vehicular speed is set to86.4km/hour, and the corresponding maximum Doppler frequency is $f_{dm} = 200\text{Hz}$. The pilot spacing is 8 in both frequency and time domains. The fading predictor has filter orders 3 and 20 in the frequency and time domains, respectively. The fading channel is generated by the ETSI Vehicular B model, which has six paths and rms delay spread of $4\mu s$. In the simulations, SNR is defined as $E_r/(LxN_oxR)$. Transmitted pilot energy is assumed to be equal to the average symbol energy i.e., $E_p = E_T/L$. In all simulations, the target BER is $BER_{tg} = 10^{-5}$. If not specified otherwise, the rate 2/3, 4-state optimal convolution encoder (constraint length K=2)is employed for both ABICM and BICM. The set of constellation sizes is {0,4,16,64}for all adaptive modulation methods, i.e. ABICM, uncoded adaptive modulation, and ATCM. For ATCM,1/2rate, 4-state Ungerboeck encoder [15] and set-partition method in are utilized.

B. Spectral Efficiency Comparison

Fig. 2 illustrates the dependency of the spectral efficiency on normalized spatial prediction range $f_{dm}\tau$,defined in the last paragraph of Section II-A. Observe that the spectral efficiencies of both uncoded adaptive modulation and ATCM decrease rapidly with increasing prediction range and ap-proach zero for prediction ranges above0. 4λ. On the other hand, the spectral efficiency of ABICM degrades very slowly and saturates at about 0.9 bps/Hz for long prediction ranges. Although ABICM is much less sensitive to prediction errors than other two adaptive modulation schemes, it still relies on fading prediction to maintain its performance. As shown in Fig. 4, for realistic prediction ranges of $0.2-0.3\lambda$,the LRP nearly doubles the spectral efficiency of the outdated CSI method, which uses a single noiseless fading sample delayed by the prediction range.

V. CONCLUSION

Improved ABICM Based on Expurgated Bound for Cellular Radio Orthogonal Multicarrier System was successfully implemented using MATLAB. Adaptive modulation techniques are much less sensitive to prediction error. The Exactness of Bit Error Ratio is maintained by the ABICM. Future extension of this work is to present operation of the variable rate Turbo Bit interleaved coded modulation in the fast desertion environment.

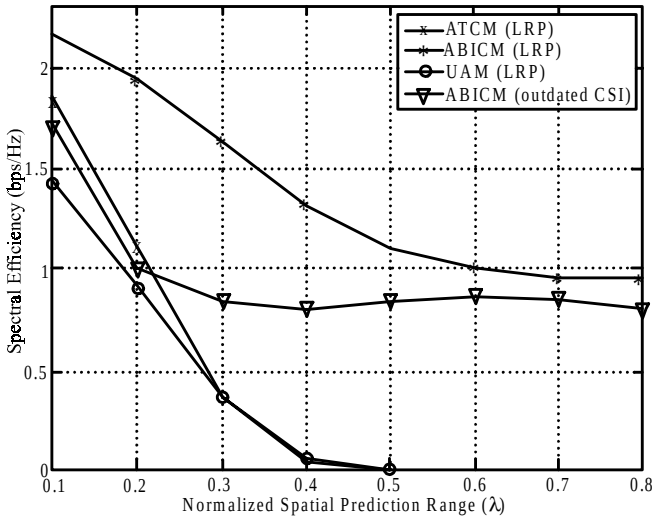

Fig. 2 : *Spectral efficiency vs. normalized spatial prediction range for SNR=15dB, ABICM, ATCM, and uncoded adaptive modulation (UAM).*

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Android Mobile Based Home Automation

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ABSTRACT

The main objective of this project is to control various home appliances using mobile phone.

Technology The main is never ending process; human beings are looking for most sophisticated embedded systems. Earlier home appliances like fan, lights, A.C and heaters etc… are switched ON and OFF mechanical and lot of physical movement is involved .in this proposed model the android mobile is used to control various home appliances and it has lot of advantages when compare to manual controlling .

Android is a software platform and operating system for mobile devices based on the Linux operating system. It allows developers to write managed code in a Java. Android application program interface (API) is designed for home automation purpose. We use BLUETOOTH communication to interface controller and android. Controller can be interfaced to the Bluetooth module through UART protocol. According to the commands received from android, the controller operates the home appliances accordingly.

This paper presents the design and implementation of a low cost but yet flexible and secure cell phone based home automation system. The design is based on a standalone microcontroller board and the home appliances are connected to the input/ output ports of this board via relays. The communication between the cell phone and the board is wireless. This system is designed to be low cost and scalable allowing variety of devices to be controlled with minimum changes to its core.

Embedded C programming is used to program ARM7 processor and keil4 is used for compilation of the embedded C code and Proteus VSM co-simulation software for Hardware verification purpose. Hardware LPC2148 is used to implement the proposed prototype.

INTRODUCTION TO EMBEDDED SYSTEMS

Embedded system overview

An embedded system can be defined as a computing device that does a specific focused job. Appliances such as the air-conditioner, VCD player, DVD player, printer, fax machine, mobile phone etc. are examples of embedded systems. Each of these appliances will have a processor and special hardware to meet the specific requirement of the application along with the embedded software that is executed by the processor for meeting that specific requirement. The embedded software is also called “firm ware”. The desktop/laptop computer is a general purpose computer. You can use it for a variety of applications such as playing games, word processing, accounting, software development and so on. In contrast, the software in the embedded systems is always fixed listed below:

Embedded systems do a very specific task; they cannot be programmed to do different things. Embedded systems have very limited resources, particularly the memory. Generally, they do not have secondary storage devices such as the CDROM or the floppy disk. Embedded systems have to work against some deadlines. A specific job has to be completed within a specific time. In some embedded systems, called real-time systems, the deadlines are stringent. Missing a deadline may cause a catastrophe-loss of life or damage to property. Embedded systems are constrained for power. As many embedded systems

operate through a battery, the power consumption has to be very low.

- Some embedded systems have to operate in extreme environmental conditions such as very high temperatures and humidity.

APPLICATION AREAS OF EMBEDDED SYSTEMS

Nearly 99 per cent of the processors manufactured end up in embedded systems. The embedded system market is one of the highest growth areas as these systems are used in very market segment- consumer electronics, office automation, industrial automation, biomedical engineering, wireless communication, data communication, telecommunications, transportation, military and so on.

* CONSUMER APPLICATIONS
* OFFICE AUTOMATION
* INDURSTAL AUTOMATION
* MEDICAL ELECTRONICS
* COMPUTER NETWORKING
* TELE COMMUNICATIONS
* WIRELESS TECHONOLOGIES
* INSEMINATION
* SECURITY
* FINANCE

INTRODUCTION TO ARM7 LPC2148

General description

The LPC2141/42/44/46/48 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine microcontroller with embedded high speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to their tiny size and low power consumption,

LPC2141/42/44/46/48 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. Serial communications interfaces ranging from a USB 2.0 Full-speed device, multiple UARTs, SPI, SSP to I2C-bus and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers suitable for industrial control and medical systems.

ARM7 LPC 2148 Introduction

The ASK 16/32-bit ARM7TDMI-S microcontroller Training board is specifically designed to help students to master the required skills in the area of embedded systems. The kit is designed in such way that all the possible features of the microcontroller will be easily used by the students. The kit supports in system programming (ISP) which is done through serial port. ASK Board has new and advance options which will give user the liberty of implementing complex logic used in the design of Embedded Systems. The development experience on the ASK Board will posed an opportunity to excel in the field of Embedded Systems.

Fig.1 : *LPC 2148Development board*

BOARD FEATURES

- Processor: LPC2148
- 2xSerial ports(One for ISP and other for Serial Communication)
- 12.00 MHz crystal
- On board Reset Circuit with a switch.
- Dual Power supply (either through USB or using external power adapter).
- Power on LED supply.
- Three on-board voltage regulators 1.8V, 3.3V and 5V with up to 800mA current
- Extension headers for µC ports.
- Graphic LDC display interfacing port.
- USB Ports.
- CAN controller interfacing.
- MMC/SD card interfacing.
- 8 Bit LED interfacing.
- EEPROM Interfacing.
- On board UART.

Android mobile/Apps

Android is a mobile operating system developed by Google. It is used by several smart phones, such as the Motorola Droid, the Samsung Galaxy, and Google's own Nexus One.

The Android operating system (OS) is based on the open Linux kernel. Unlike the iphone OS, Android is open source, meaning developers can modify and customize the OS for each phone. Therefore, different Android-based phones may have different graphical user interfaces GUIs even though they use the same OS.

Android phones typically come with several built-in applications and also support third-party programs. Developers can create programs for Android using the free Android SDK (Software Developer Kit). Android programs are written in Java and run through Google's "Davlik" virtual machine, which is optimized for mobile devices. Users can download Android "apps" from the online Android Market.

Since several manufacturers make Android-based phones, it is not always easy to tell if a phone is running the Android operating system. If you are unsure what operating system a phone uses, you can often find the system information by selecting "About" in the Settings menu. The name "Android" comes from the term android, which refers to a robot designed to look and act like a human.

HARDWARE IMPLEMENTATION

Bluetooth is a proprietary open wireless technology standard for exchanging data over short distances from fixed and mobile devices, creating personal area networks (PANs) with high levels of security. Bluetooth technology allows electronic devices to communicate wirelessly.

GSM is a digital mobile telephony system. GSM digitizes and compresses data, then sends it down a channel with two other streams of user data, each in its own time slot. It operates at either the 900 MHz or 1800 MHz frequency band.

The temperature sensor LM35 senses the temperature and converts it into an electrical signal, which is applied to the micro controller through ADC. The analog signal is converted into digital format by the analog-to-digital converter (ADC). The sensed values of the temperature are displayed on the UART.

HARDWARE REQUIREMENTS

- LPC2148 Development kit
- GSM Module
- BLUETOOTH with Receiving Section
- Buzzer
- LM35(Temperature measurement)

SOFTWARE IMPLEMENTATION

To compile the above C code you need the KEIL software. They must be properly set up and a project with correct settings must be created in order to compile the code. To compile the above code, the C file must be added to the project.

In Keil, you want to develop or debug the project without any hardware setup. You must compile the code for generating HEX file. In debugging Mode, you want to check the port output without LPC2148 Evaluation Board.

The Flash Magic software is used to download the hex file into your microcontroller IC LPC2148 through UART0.

SOFTWARE REQUIREMENTS

- KEIL4 Micro vision with Embedded 'c'
- Proteus(Testing Hardware)
- Flash Magic(Synthesis)

HARDWARE INTEGRATION

To compile the both hardware and software is verified.

CONCULSION

This paper presents the design and implementation of a low cost but yet flexible and secure cell phone based home automation system. The design is based on a standalone microcontroller board and the home appliances are connected to the input/ output ports of this board via relays. The communication between the cell phone and the board is wireless. This system is designed to be low cost and scalable allowing variety of devices to be controlled with minimum changes to its core.

Embedded C programming is used to program ARM7 processor and keil4 is used for compilation of the embedded C code and Proteus VSM co-simulation software for Hardware verification purpose. Hardware LPC2148 is used to implement the proposed prototype.

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Real Time Moving Object Tracking in GPS and Zigbee

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ABSTRACT

In the past, the real-time tracking of vehicles, items, and personnel was only a Reality for large government agencies in spy novels. Recent developments in technology are now bringing this type of tracking capability to the general public. Real-time tracking Systems could be used to monitor the locations of police squad cars and ambulances for faster emergency response time. The location of public transportation vehicles, such as buses could be displayed at bus stop terminals for interested patrons. In this project tracking the missing or kidnapping persons/ animals, mentally retarded persons by using Zigbee and GPS.

ZIGBEE measure the signal strength of the received data. This technology can help us to implement a low-cost, low-power location monitoring system for indoor environments where other positioning systems have typically performed poorly. This article is a useful tool to help system designers understand the very basic concepts of cooperative localization. Zigbee acts as both Transmitter and Receiver. GPS receive satellite signals and calculate coordinates. It is a space-based satellite navigation system that provides location and time information in all weather conditions, anywhere on or near the Earth where there is an unobstructed line of sight to four or more GPS satellites. The system provides critical capabilities to military, civil and commercial users around the world. GPS devices provide latitude and longitude information.

The aim of the project is to tracking Humans/animals which is in the specified range. This is an old technique already employed and in use but the new thing about this project is using an advanced wireless protocol device called ZIGBEE along with GPS. Zigbee acts as both Transmitter and Receiver. The purpose of Human Tracking for improving accuracy is to provide a better service to tracking people and observing obstacle will be more useful for Security in known and unknown environments, Safety for a Humans and Animals. The proposed project will be utilizing this technology tracking system for Humans such that the position of the Human is detected by utilizing Zigbee and GPS communication. In this project the tracking is done depending on the feedback signal provided by the Zigbee communication, which is the core part of this project. A coordinator is taken the data from end device and identifies the person/animal location by using Google Earth.

Index terms- Zigbee, tracking, GPS, topology, Mesh

OBJECTIVE

- Studying GPS and Zigbee.
- Studying National Marine Electronics Association (NMEA) data.
- Studying protocols i.e., Mesh, Peer-to-Peer, Broadcasting
- Studying Software.
- Calculate Accuracy.

1. INTRODUCTION

EMBEDDED SYSTEMS

Embedded systems are designed to do some specific task, rather than be a general-purpose computer for multiple tasks. Some also have real time performance constraints that must be met, for reason such as safety and usability; others may have low or no performance requirements, allowing the system hardware to be simplified to reduce costs.

An embedded system is not always a separate block - very often it is physically built-in to the device it is controlling. The software written for embedded systems is often called firmware, and is stored in read-only memory or flash convector chips rather than a disk drive. It often runs with limited computer hardware resources: small or no keyboard, screen, and little memory.

Wireless communication has become an important feature for commercial products and a popular research topic within the last ten years. There are now more mobile phone subscriptions than wired-line subscriptions. Lately, one area of commercial interest has been low-cost, low-power, and short-distance wireless communication used for \personal wireless networks." Technology advancements are providing smaller and more cost effective devices for integrating computational processing, wireless communication, and a host of other functionalities. These embedded communications devices will be integrated into applications ranging from homeland security to industry automation and monitoring. They will also enable custom tailored engineering solutions, creating a revolutionary way of disseminating and processing information. With new technologies and devices come new business activities, and the need for employees in these technological areas. Engineers who have knowledge of embedded systems and wireless communications will be in high demand. Unfortunately, there are few adorable environments available for development and classroom use, so students often do not learn about these technologies during hands-on lab exercises. The communication mediums were twisted pair, optical fiber, infrared, and generally wireless radio.

2. ZIGBEE

ZigBee is an specification of a joint of high level wireless communication protocols based on the wireless personal area network (PAN) standard IEEE 802.15.4. Its goal is the applications that require reliable communications, due to mesh topology, with low data transmission rate and long live batteries.

ZigBee can be used in several types of applications as automation and security control, control of end devices as mouse or keyboards, remote control of electronic devices, monitoring patients or elderliness but the main and most successful is home automation.

Figure 1: *ZigBee main applications.*

The characteristics that make it so suitable for these purposes are:

Low-cost - ZigBee devices are cheap as they do not need a high data rate and the microprocessor required for ZigBee devices is quite simple, due to the small size of the ZigBee MTU (Maximum Transmission Unit).

Mesh topology - Provides a higher reliability because multiple transmission paths exist. This allow some nodes of the network to be asleep while others take the control of the propagation and avoid a whole network to block if ones node gets down.

Low power consumption - As multiple nodes can be asleep until they receive some information, they do not consume too much power and the batteries can live even for 5 years.

Main Characteristics

1. It operates in the industrial, scientific and medical (ISM) bands: it can operate globally in the 2.4 GHz frequency, but also in 868 MHz (Europe) and 915 MHz (USA).
2. Its data rate is 250 kbps at 2.4 GHz, 20 kbps at 868 MHz and 40 kbps at 915 MHz.
3. Its reach range is from 10 m to 1000 m.
4. It operates over 16 channels in 2.4 GHz and over 11 channels in 868 and 915
5. MHz
6. A ZigBee network can have a maximum of 255 nodes, which mostly of time are asleep

Specifications of series2

Performance

* Indoor/urban Range- up to 133ft. (40m)
* Outdoor RF line-of-sight Range- up to 400 ft. (120m)
* Transmit Power output (software selectable)- 2mW (+3dBm)
* RF Data Rate- 250,000 bps
* Serial Interface Data Rate(software selectable)- 200-23400 bps (non-standard baud rates also supported)
* Receiver Sensitivity- -95 dBm (1% packet error rate)

Power Requirements

* Supply voltage- 2.8-3.4V
* Operating current (Transmit)- 40mA (@3.3 V)
* Operating current (Receive)- 40mA (@3.3 V)
* power-down Current- <1 uA @ 25^{o} c

General

* Operating Frequency Band- ISM 2.4 GHZ
* Dimensions- 0.960" x1.087" (2.438cm x 2.761cm)
* Operating Temperature- -40 to 85^{o} C (industrial)
* Antenna Options- Integrated whip, chip, RPSMA, or U.FL Connector

Networking & Security

* Supported Network Topologies- Point-to-point, point-to-multipoint, Peer-to-peer & Mesh
* Number of Channels (software selectable)- 16 Direct Sequence Channels
* Addressing Options- PAN ID and Addresses, Cluster IDs and end points (optional)

Device types

There are three different types of ZigBee devices:

ZigBee coordinator (ZC) **:** The most capable device, the coordinator forms the root of the network tree and might bridge to other networks. There is exactly one ZigBee coordinator in each network since it is the device that started the network originally. It is able to store information about the network, including acting as the Trust Centre & repository for security keys.

ZigBee Router (ZR) **:** As well as running an application function, a router can act as an intermediate router, passing on data from other devices.

ZigBee End Device (ZED): Contains just enough functionality to talk to the parent node (either the coordinator or a router); it cannot relay data from other devices. This relationship allows the node to be asleep a significant amount of the time thereby giving long battery life. A ZED requires the least amount of memory, and therefore can be less expensive to manufacture than a ZR or ZC.

TOPOLOGIES

ZigBee allows three different topologies

Point to point: In this topology, it has only Coordinator and End Device. It can communicate one to each other.

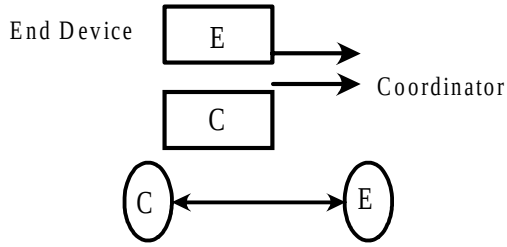

Figure 2(a): *Point-to-point*

Star topology: The Coordinator is in the middle and all the rest of devices are connected to it. If the coordinator blocks, no node is able to continue communicating with another node.

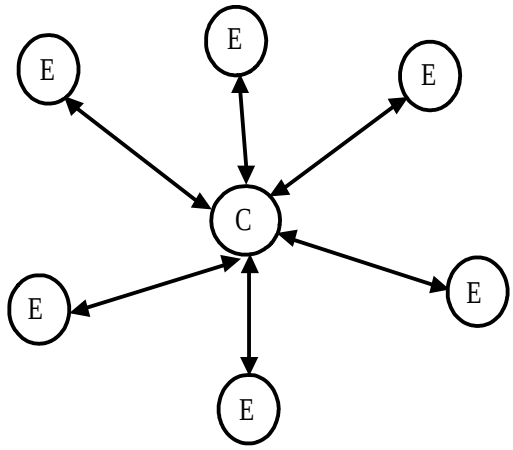

Figure 2(b) : *Star network*

Mesh network: In a Mesh network, such as Zigbee, devices have one of three different duties:

- Coordinator: It establishes and maintains the network by assigning addresses to joining (associated) devices and assisting with route building.
- Router: move data between nodes that cannot communicate directly due to distances.
- End points: The node that collects data and controls devices on the network and it is typically connected to our controllers, sensors and other devices for network interfacing.

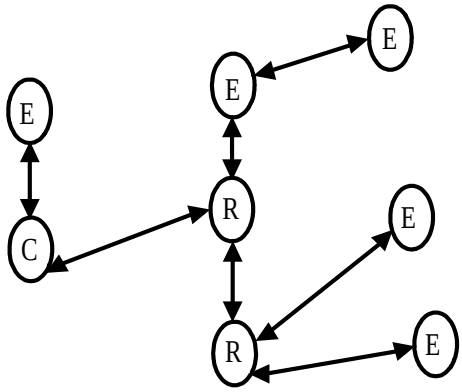

Figure 2(b) : *Mesh Network*

ZigBee Applications

ZigBee enables broad-based deployment of wireless networks with low-cost, low-power solutions. It provides the ability to run for years on inexpensive batteries for a host of monitoring applications: Lighting controls, AMR (Automatic Meter Reading), smoke and CO detectors, wireless telemetry, HVAC control, heating control, home security, Environmental controls and shade controls, etc

3. HARDWAREIMPLEMENTATION

The proposed system is real time person location detection and tracking system using Global Positioning System (GPS) module, and Zigbee modules. In this system, each person is required to carry a match box-size device, which consists of Zigbee module and GPS receiver. At the tracking side there will be Zigbee module and PC, Google earth software. Whenever we want to track a person we will send a request to corresponding tag, the tag sends GPS data to the Receiver. Using this information Google earth will detect and track that person.

In order to relate the project objective the following H/W and S/W's are used.

a. GPS

b. Zigbee Module.

c. PC.

d. Google Earth Software.

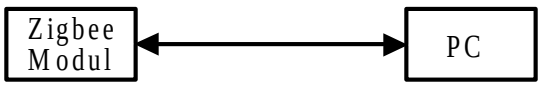

Figure 3(a) : *Tracking Module*

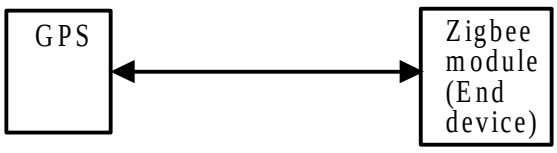

Figure 3(b) : *Radio Tag*

Global Positioning System (GPS)

GPS receives the GPS data from Satellites which covers the entire earth. This will be send to tracking module through Zigbee module.

Zigbee Module

XBee and XBee-PRO 802.15.4 OEM modules are embedded solutions providing wireless end-point connectivity to devices. These modules use the IEEE 802.15.4 networking protocol for fast point-to-multipoint or peer-to-peer networking. The zigbee module at transmitter side transmits the request to tag and receives the GPS data from tag. The Zigbee at the tag receives request and transmits the GPS data to tracking module.

4. GLOBALPOSITIONING SYSTEM

GPS Background Information:

The Global Positioning system (GPS) is a space –based global navigation satellite system (GNSS) that provides reliable location and time information in all weather and at all times and anywhere on or near the earth when and where there is an unobstructed line of sight to four or more GPS satellites. It is maintained by anyone with a GPS receiver.

GPS was created and realized by the U.S. Department of Defense (USDOD) and was originally run with 24 satellites. It was established in 1973 to overcome the limitations of previous navigation systems.

In addition to GPS other systems are in use or under development. The Russian Global Navigation satellite (GLONASS) was for use by the Russian military only until 2007. There are also the planned Chinese Compass navigation system and Galileo positioning system of the European Union (EU).

BASIC CONCEPTS OF GPS

A GPS receiver calculates its position by precisely timing the signals sent by GPS satellite high above the Earth. Each satellite continually transmits messages that include

1. The time message was transmitted.
2. Precise orbital information.
3. Generally system health and rough orbits of all GPS satellite (the almanac).

The receiver uses the messages it receives to determines the transmit time of each message and computes the distance to each satellite. These distances along with the satellites locations are used with the possible aid of trilateration, depending on which algorithm is used, to compute the position of receiver. This position is then

displayed, perhaps with a moving map display or latitude; elevation information may be included. Many GPS units show derived information such as direction and speed, calculate from position changes.

Three satellites might seem enough to solve foe position since has three dimensions and a position near the Earth's surface can be assumed. However, even a very small clock error multiplied by the very large speed of light, speed of which satellite signals propagate results in a large positional error. Therefore receivers use four or more satellites to solve for the receivers location time and date.

For as long as man has been on this earth, he has been searching for accurate navigation and positioning methods; from the first man travelling on foot and using landmarks to determine his position, to a SR-71 Blackbird military aircraft gathering target location data while travelling at supersonic speeds. The United States Department of Defense runs a freely available and highly accurate positioning system called GPS.

5. CONCLUSION

In this paper we have research several papers to know the recent development in the field of tracking. All the methods are using any interfaces like microcontroller or microprocessor.This paper presents our work for Normal Human Tracking and mentally retarded Person Tracking based on Zigbee and GPS. With the help of Zigbee, GPS and GOOGLE earth software we track the person even if the person inside the room. By using Mesh topology we have to extend the range also.

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Performance of bit - interleaved coded multi - antenna OFDMA systems over space - frequency selective fading channels

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ABSTRACT

Multiple (MIMO) antennas of input multiple output systems with orthogon frequency division multiple access (OFDMA) is the most promising combinati of technologies for broadband services in wireless networks to next generation. Performance monitoring of multicellular systems based on these technologies is essential to provide broadband wireless standards such as WiMAX and 3GPP LTE. In this article, we define an analytical framework to evaluate the probability of error of average convolution MIMO OFDMA multi-coded bit-interleaved systems. Mitigation strategies multiuser interference both random and coordinated access account. In this scenario, the analysis of the correlation of the channel fading in the frequency domain space and possible non-stationary properties of the multi-cell interference framework should (per subcarrier randomization). The analysis is performed for various multi-antenna carried strategies from the beam forming associated containment outside the cell patterns on orthogonal spatial diversity space-time coding is based disorders. The numerical results confirm the analytical framework proposed for heterogeneous and a wide range of system configurations environments.

Index Terms

MIMO, OFDM, bit-interleaved coded modulation (BICM), beamforming, OSTBC, interference management, effective SINR, WiMAX, LTE, LTE advanced.

I. INTRODUCTION

Orthogonal Frequency Division Multiple Access (OFDMA) wireless systems are the next generation is chosen for its flexibility and scalability. This is driving the demand for the services of broadband for high throughput makes OFDMA with multi-antenna (or Multiple Input Multiple Output - MIMO) systems in the most efficient and flexible solution for high standards of spectral efficiency. Today, several commercial solutions, using OFDMA technology development, such as the IEEE global interoperability for Microwave Access (WiMAX) [1] and the Long Term Evolution (LTE) project of the 3rd Generation Partnership (3GPP) [2]. This system of high data rates are expected to operate in heterogeneous environments. The interference mitigation and channel aware scheduling algorithms are essential to make the most of their ability. [3]

Power control is required for setting the system parameters, but the wide range of propagation scenarios / possible interference and cell deployments is this analysis a very complex task. Analytical models for the performance of the physical layer (although simplified settings) are relevant to reduce the computational load of extensive simulations. To be useful, the framework of analysis for the main system parameters such as multistage scenarios with convenient access multi-user and channel models / realistic political interference, multi-antenna links with bit-interleaved coded modulation (BICM) and your account must be orthogonal frequency division multiplexing (OFDM) in the space-frequency-fading channels. [4] In addition, cellular systems are affected by interference caused by non-stationary fluctuations of the traffic load in the cell, the performance analysis of interference mitigation and adaptive modulation coding techniques. Although performance analysis on fairly well established MIMO fading channels [5] - [6], a realistic assessment of analytical performance models must be adapted to allow these features to take into account the cellular wide band practices .

A. Background on OFDM performance assessment

The historic route sheet [7] comes from the early 60s with the idea of using frequency division multiplexing with overlapping sub-channels [8], the OFDM system as we see it today. [9] During the 80 and 90 codes OFDM (COFDM) for Digital Video Broadcasting (DVB) was the first massive application studied [10] - [13]. COFDM for cellular mobile radio systems with driver-based correction was proposed by [14]. Codeword interleaving and frequency over time have proven to be an effective solution in selective Rayleigh channels in [15]. A general framework for performance evaluation of BICM was given as theoretical analysis of information on the channel capacity and the cutoff frequency function. The average time to failure and services for a wide range of digital communication systems are presented in [4], where multi-antenna and propagation environments combined fading techniques were considered. In addition, the effects of fluctuations due to the depreciation of non-stationary noise were treated.

COFDM is today at the heart of most communication standards physical layer such as WiFi , WiMAX [1] and LTE [2]. Recently, research has focused strategies and achievements on the derivation of analytical tools for the evaluation of different configurations of system time. The error rate of the slot in clear channel selective fading nonlinear frequency is derived from the DVB systems. In the analytical study has been adapted for the bit error rate coded for DVB systems. Deposit for frequency selective channels, the signal-to-noise efficient (SNR) in that the SNR of (AWGN) channel frequency corresponding flat additive white Gaussian noise, the same elastic power. The idea of ??the effective SNR is simple, but powerful to assess the modulation and coding instantaneous channel conditions (and service requirements), or to adjust the average error rate for a particular mode of transmission. The recent approach in exponential effective SNR mapping (EESM) which provides a semi-analytical model of the performance of the bonding layer COFDM systems developed , extensions of WiMAX and LTE. The MSET and ESM method based on mutual information represents the current performance of these systems for a response frequency selective channel data and the average configuration without interference on fading and interference statistics. In some cases, they are practical and easy to implement fairly accurate, but they still need to simulate the propagation environment of the chain and some adjustments in the context of numerical simulations. In the statistics of the effective SNR come from multi-antenna WiMAX systems in fading environments to estimate the average error rate without these heuristics adjustments. This paper is the analysis of systems with multiple antennas at both links, non-stationary intercell interference and higher order modulations.

B. Original contributions

In this paper, we propose a new method to evaluate the performance of MIMO-OFDMA systems on space-channel frequency-selective and non-stationary noise. Performance is evaluated in terms of average bit error rate at the output of the error correction (FEC) decoder before. We focus on the convolution coding scheme. FEC required for the majority of commercial standards with BICM OFDM Technology However, the analysis of the related compound approach is general and can be block or convolutional code can be extended. To give a brief overview of the proposed methodology, we consider the transmission of a code word on a number of parallel sub-channels (ie, the OFDM subcarriers). The performance of the coded, deriving the pairwise error probability (PEP) bound for the code word transmitted by the terminal connection to consider. PEP, say (*c*) *c* error for the event depends on the statistics of random signal to interference plus noise ratio (SINR) variables that are experienced across sub-channels *c*. Let γ *k* as SINR value associated with the *k* the sub channel and $\gamma = \gamma k\}$ {the set of all SINR. Due to multipath and interference over time to neighboring cells, SINR values are random variables γ, the statistical characteristics of the fading channel and the interference level ٦ H along sub channels observed in the correlated part. The contribution of this work is the calculation of the average probability of error as follows:

$$p(c) = E_{\gamma}[p((c \mid \gamma))] \quad \text{.....(1)}$$

Taking into account the statistical properties of H and ٦ The mean is the first in terms of the way spatio-temporal correlation (*H* E [.]) by deriving the probability density function of the effective SINR (pdf) and then to compared to the disturbance produced configuration (E *I* [.]) according to the guidelines the analysis is for MIMOOFDMA scenarios with different system parameters such as transmission modes paid (eg, modulation, interleaving, programming multi-cell setting page, scheduling strategies), the multi-processing systems -antennas (such as beamforming, diversity) and propagation environments. According to the IEEE 802.16d / e and protocols 3GPP LTE air, we transmission patterns conform to either coordinated or random interference scenarios.

The analysis focuses on two relevant fading and interference mitigation strategies: i) outside antenna beamforming treatment for mitigation of extracellular interference coupled closely together, and ii) widely separated antennas orthogonal space-time block coding (OSTBC distance) to obtain spatial diversity. The analysis takes into account the correlation of the channel on the subcarriers (due to multipath) and antennas (in the case of closely spaced antennas) and the inter-cell interference non-stationary (due to multi-user policy and the scheduling strategy adopted by cells).

The paper is organized as follows. The model of multi-cell MIMO OFDMA system is described in Sec. II-A. Interference of multi-user access and the corresponding scenario in Sec. II-B. Signal model and receiver configurations are detailed in Sec. II-C, while the statistical properties of the channel and the interference Sec.II-D. Specific scenarios are used for performance analysis, presented in Sec. III of the analytical framework is derived in Sec. IV-V. A numerical validation for WiMAX IEEE 802.16d / e and 3GPP LTE systems is presented in Sec. VI.

II. SYSTEM DEFINITION

A. OFDMA cellular layout

We consider a scenario OFDMA cellular communication as shown in 1 for uplink (justification for the downlink would be similar, see chap. VI). Is provided in each cell of the base station (BS) with $\geq$ 1 N_R antennas and each subscriber stations (SSS) have n_T antenna array elements $\geq$ 1. The transmission is organized in accordance with the logical frame structure of FIG. 1 observed $K\ T\ Z$ adjacent subcarriers on successive OFDM symbols. In each cell is the multiple access the logical framework (data area) of each subcarrier $\times\ K\ Z$ treated in time-frequency units. The BS may assign one or more data fields on each SS.Multi-user scheduling strategy, the rule of mapping the logical framework for natural resources to form the physical time-frequency frame. As some of subcarrier can be empty, the traffic load $\eta \leq 1$ is introduced to indicate the number of subcarriers of total assets.

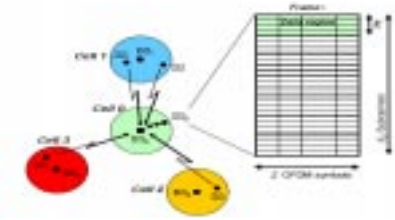

Fig. 1. Example of interference scenario in a multi-cell system (uplink) where transmission is based on a frame structure composed by data regions. The user SS0 shares the same radio resources of the interfering users highlighted in the nearby cells.

Examine the relationship between a subscriber station and say SS0 own base station, BS0, data on a single region with indices physical subcarriers associated $K = \{k$ 1. . . , With ki} $K\ k$ travels KT subcarriers for data transmission. SS0 to transfer BS0 is altered by the intervention of n_i used SSs around cells that share some (or all) of the time-frequency resources SS0 (see example in Fig. 1). For simplicity, all the cells are expected to adopt the same partition resources in terms of organization of the logical framework and the scheduling strategy. All cells are synchronous frame (asynchronous cell expansion chassis would analytically tedious but conceptually simple) so as to by an interfering cell (referred SS0 interfering cell for i-th) of each may be active OFDM subcarrier. The number of users affected by the transmission on each subcarrier SS0 is a random variable, the load from 0 to full N_i for $\eta = 1$

B. Multi-user access scenarios

Several rules for multi-user access can be adopted for different user data are assigned to time-frequency resources. Planning specifies the mapping between the regions of control logic data and physical resources to cope with fading over time and interference. Conventional techniques adopted scheduling in OFDMA systems (eg, IEEE 802.16 WiMAX and 3GPP LTE is based on two coordinated policies or random multi-user access.

For each sub - carrier mapping of logical data area in adjacent parts of the spectrum available to coordinate access. The mapping rule is the same for each cell, wherein the user data in the cell fully integrated into the data area by another user in a neighboring cell when the two base stations ovelaps program preset to subscriber on the same data area. H. can vary depending on the degree of cooperation between BSS and the traffic load of each interfering field experiences with constant power over the entire surface of the NI data. Figure -2 a shows the concept CELL0 perspective from both BS1 and BS3 on the same data area is provided CELL0 independent access, is the use of two cells of the total area of fixed data.

Unlike coordinated approach employs interference randomization, a cell specific policy permutation bandwidth of the subcarrier before OFDMA subcarrier mapping logic physical resources in order randomization of interference in the single data field. The scheduler allocates subcarriers of the logical part of physical subcarriers according to a pseudo-random permutation of the transmitter and receiver generally known.

Figure. 2-b shows the effect of the permutation of the cell arrangement shown in figure. 1 product, highlighting the randomness of disorder on the subcarriers of the data area of logic 1 for the 0th cell can be noted that all SS interfere SS0 changes subcarriers to subcarriers and number of varied randomly from 0 to traffic load $\eta \leq 1$ OR jammers. These non-stationary artificially created to induce diversity against interference. Similar to the coordinated access the randomized approach adopted as encryption of data in the frequency domain, so that the interference patterns are assumed to be constant over the symbols Z frame.

In this work, we consider both the coordination and policy random scheduling in the uplink case. Note that the previous policy of each BS scheduler can dynamically optimize the allocation of a certain data range to minimize cross-interference. However, since the optimization of the scheduler is not the subject of this document are the assignments of data areas are assumed here randomly and independently from one cell to a non-optimized scheduler

C. Signal model

The diagram of FIG. Figure 3 shows the configuration of the transmitter and receiver to connect SS0-BS0. A sequence {bk} bits by a convolutional code (CC) to rate Rcc = KCC / Ncc coded. The codeword is then interleaved and mapped to complex-valued symbols {xk}, which, in a set S = {s_1 modulation ..... S_m} are defined dimension M = 2m. Modulated signals xk ? S are assigned to the logical data area is assigned to the user SS0 and then mapped to the physical resources of the chassis under the random or coordinated scheduling strategy. Each OFDM symbol of the frame is affected by the transferred using a frequency selective fading channel with Gaussian multi-antenna system, and the inter-cell interference. Channel fading and interference can be assumed to be constant in a frame, but varies from frame to frame (block fading channels).

Without loss of generality, we can now focus on one OFDM symbol frameN_R X1. The baseband signal is obtained on sub-carrier i-th, as a model

$$y_k = \sqrt{p_o} H_k x_k \qquad .....(2)$$

Where the transmitting power is indicated with P0, the $N_R \times N_T$ MIMO matrix **H***k* gathers the complex channel gains and the $N_T X1$ vector x_k collects the transmitted symbols mapped over the antennas with normalized energy

$$E[\| x_k \|]^2 = 1.$$

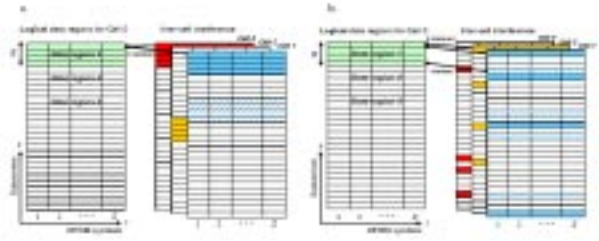

Fig. 2. Example of multi-user access policies applied to the cellular layout of Figure. 1. For the coordination approach (a) each data region is mapped onto a set of contiguous subcarriers, so that the out-of-cell interference can be assumed stationary along the data regions. In case of randomization (b) the subcarriers of each data region are spread all over the bandwidth according to a different pseudo-random permutation rule in each cell leading to non-stationary interference.

The subcarrier index $k \in K$ ranges over the k allocated subcarriers. The $N_R X1$ vector models the background noise and the co-cell interference on the i^{th} subcarrier as Gaussian with spatial correlation

$$Q_k = \sum_{i=7_k} P_i Q_{K,i} + \sigma^2_{bn} I_{NR} \qquad .....(3)$$

Background noise has power σ^2_{bn} . The interfering signal from the i^{th} cell is characterized by a transmitting power *a*nd a spatial covariance Q_k , that remains the same over a number of frames since it is related to the spatial position of the interfering users. The covariance matrix is normalized with $[Q,k,i]_{nR,nR} = 1$ for nR = *{*1, . . ., N_R *}*. Let us label with index i = 1. . . N_I the interfering cells, the set $\gamma_k \subseteq 1,\ldots, N_1$ denotes the group of cells that are using the same i^{th} subcarrier as SS0. The cardinality

$V_k = |\gamma_k| \in \{0,\ldots \ldots \ldots N_1\}$ gives the number of active interferers while the set γ_k depends on the index *k* as the configuration of the interferers varies along the subcarriers according to the adopted interference management policy. After physical-logical demapping, the received signals **y***k* are processed by the multi-antenna combiner (see Fig. 3) according to the channel state information (CSI) that includes both channel and interference conditions. The combiner provides the estimates x_k of the transmitted symbols paired with the corresponding SINR values $\gamma_k = \gamma_k(H_k, \gamma_k)$ Max-Log-

Map demodulation is carried out to provide the log-likelihood ratios (LLR) to the Viterbi decoder. For LLR computation the instantaneous channels **H***k* are assumed to be perfectly known while the interference levels N_1 (that may rapidly vary with k due to subcarrier permutation) are known either perfectly or in average only.

D. Channel and interference model

In frequency-selective multipath environment, the $NR \times NT$ channel response **H***k* on the *i*th subcarrier can be modeled as the sum of W path contributions:

$$H_k = G_k \sum_{\gamma=1}^{W} \sqrt{P_r} A_\gamma \exp\left(-2\pi \frac{k}{N}\right) \quad .....(4)$$

Where each path is characterized by mean power P_r, the $NR \times NT$ fading amplitudes. The complex term G_k denotes the frequency response of the cascade connection of the transmitter and receiver filters on the ith subcarrier, The fading amplitudes (are assumed to be Rayleigh distributed and uncorrelated from path to path, according to the wide sense stationary uncorrelated scattering model:

$$R_{S.\gamma} = R_{TX,\gamma} \otimes R_{RX,\gamma} \quad .....(5)$$

accounts for the spatial correlation of the fading channel, denoting the Kronecker product and with $\mathbf{R}_{TX}$, and $\mathbf{R}_{RX}$, being the spatial covariances among the transmitting and receiving antennas respectively. We consider two different models corresponding to different assumptions about correlation (5) and geometry of the antenna arrays: a beamforming model is adopted for antenna arrays with closely spaced apart elements and a diversity model for array elements that are sufficiently far apart.

1) **Beamforming (geometrical) model :** For the beamforming case the r^{th} path can be described by a direction of departure $\theta_\gamma^{(T)}$ (DOD), a direction of arrival $\theta_\gamma^{(R)}$ (DOA) and a complex fading term α_γ with $E\left[\| \alpha_\gamma \|\right]^2 = 1$. Let the NT × 1 vector $a_T\left(\theta_\gamma^{(T)}\right)$ denote the response of the SS antenna array to the DOD $\theta_\gamma^{(T)}$, the NR × 1 vector $a_R\left(\theta_\gamma^{(R)}\right)$ is the response of the BS antenna array to the DOA $\theta_\gamma^{(R)}$, the beamforming model yields $Ar = \alpha_\gamma a_R\left(\theta_\gamma^{(R)}\right) a_T\left(\theta_\gamma^{(T)}\right)$ with correlation matrices $R_{TXr} = a_T\left(\theta_\gamma^{(T)}\right) \quad a_T^H\left(\theta_\gamma^{(T)}\right)$ and

$$R_{RXr} = a_R\left(\theta_\gamma^{(R)}\right) a_R^H\left(\theta_\gamma^{(R)}\right)$$

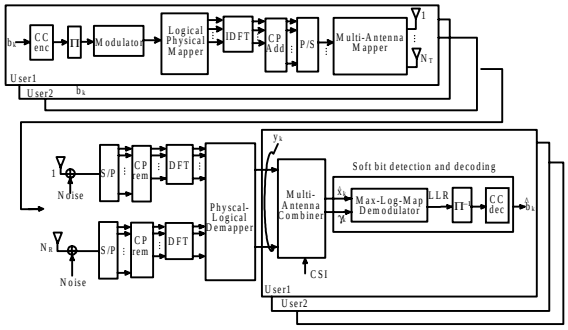

Fig. 3 : *Transmitter and receiver block diagram.*

A similar model is employed also for the covariance matrix of the interfering signal from the rth cell:

$$Qk,i = \sum_{r=1}^{W} pi, ra R\left(\theta_r^{(R)}\right) aRH\left(\theta_r^{(R)}\right) \quad .....(6)$$

Which depends on the DOAs $\left(\theta_r^{(R)}\right)$ and the fading power profile $|\overline{\tau_k}|$ $\left(\theta_r^{(T)}\right)$ of the r^t interferer, here modeled with W_I path contributions. The power profile is normalized to one,. The overall interference covariance **Q** is obtained according to (3):

$$Q_k = \sum_{i=7_k} P_i \sum_{\gamma=1}^{W} pi, \gamma aR\left(\theta_\gamma^{(r)}\right) aRH\left(\theta_\gamma^{(R)}\right) .....(7)$$

By combining the covariances (6) with the powers *pi* for those interferers that are active on the r^{th} subcarrier according to the scheduling policy.

2) **Diversity model :** For rich scattering environments the received fading signals are uncorrelated among the antennas, so that Rs,r, = $I_{NR,NT}$ $Q_{k,I,} = p_i I_{NR}$ and thus $Q_k = \sigma_{bn}^2 I_{NR}$ The total interference power measured on the k^{th} subcarrier is

$$\sigma_k^2 = \sum_{i \in 7_k} P_i + \sigma_{bn}^2 \quad .....(8)$$

based on the assumption that all the interferers have the same transmitting power (but they can be active or not according to the scheduling policy).

III. SCENARIOS FOR PERFORMANCE ASSESSMENT

In this section, we define two specific performance evaluation scenarios. If interference is spatially correlated (§ II-D1), the covariance matrix (7) and structured so that the multi-antenna combination can use this knowledge to reduce the inter-cell interference of a training strategy appropriate beam. By filtering with policy formation beams scheduling coordinate system in pairs as in the present inter-cell interference, the spatial structure of the interference

remains the same over the entire range of data with many practical advantages (example, the interference covariance must be estimated with high accuracy). Correlate the other hand, the disorder, such as the variety of model (Section II-D2) coupled to the politics of the time / space / use maximum interference diversity random scheduling. Even if the noise power subcarrier changed to the subcarrier according to (8), wherein the receiver may be realistic, the average noise power in the data area K, σ^ 2 = 1/KZ ∑_ (k ? K) ? σ_k ^ 2 is the interference level used in soft decoding. Based on these considerations, we define the following two typical scenarios

Coordinated interference scenario : In the coordinated strategy, the data regions in all cells are mapped over adjacent, or piecewise-adjacent, subcarriers which make the interference pattern to be constant over the whole data region and thus $Q_k = Q$, for $k \in K$. The stationary of the interference configuration allows for an accurate estimate of the impairment covariance **Q** which can be efficiently exploited for *interference mitigation*. The MIMO-OFDMA system provides two dimensions that can be employed for interference reduction: the frequency domain of the OFDM signaling and the spatial domain offered by the array processing. To enhance the interference rejection capability, we adopt a uniform linear antenna array (ULA) with closely spaced apart antennas and a beamforming processing over each subcarrier. The SINR variate $\gamma_k = \gamma(H_k, \Gamma)$ depends only on the channel variations over k, whereas the interference pattern Γ does not vary along the data region. Assuming the perfect knowledge of $\{H_k, Q\}$, the minimum variance distortionless receiver (MVDR) is used to combine the signals received at different antennas, yielding at the output of the combiner the following SINR.

$$\gamma_k = \frac{p_o}{N_T} t\gamma\left\{H_K^H Q^{-1} H_K\right\} \qquad .....(9)$$

to be exploited when establishing the branch metric of the Viterbi decoder. The channel **H** and the interference covariance **Q** of this scenario are modeled according to the beamforming model described in Sec. II-D1.

Randomized interference scenario : This scenario is modeled to exploit the *maximum diversity* provided by the fluctuations of both channel and impairments. Diversity is artificially introduced through the randomized multi-user access approach which provides interference fluctuations over the codeword. In this case, any interference mitigation techniques is unfeasible due to the unpredictability of the impairments configuration (i.e., the highly varying covariance **Q** cannot be reliably estimated). To exploit the diversity provided by the MIMO channel we adopt an OSTBC with antennas sufficiently spaced apart. The receiver is based on coherent maximum likelihood (ML) OSTBC detector as described , where the Viterbi decoder exploits the knowledge of the average noise power σ^{-2} over the whole data region (*conventional decoder*). In this case, the SINR to be used for decoding is

$$\gamma_k = \frac{p_o}{N_T} \frac{t\gamma\left(H_K^H Q^{-1} H_K\right)}{\sigma^2} \qquad .....(10)$$

As lower-bound performance reference, we also consider the optimal decoding based on the knowledge of the instantaneous interference power σk^2 on each subcarrier for this genie decoder the instantaneous SINR at the decision variable is

$$\gamma k = \frac{p_o}{N_T} \frac{t\gamma\left(H_K^H Q^{-1} H_K\right)}{\sigma k^2} \qquad .....(11)$$

The channel and the interference are modeled as described in Sec. II-D2. For analytical purposes, it is convenient to rewrite the SINR as a function of the $N_T N_R \times 1$ normalized space-frequency channel vector

$$h'_k = \sqrt{\frac{p_0}{N_T}}.vec\left(Q_k^{-H/2} H_K\right) \qquad .....(12)$$

Where the interference covariance is $Q_k = Q$ defined as in (7) for the coordinated scenario, $Q_k = \sigma^2 I_{NR}$ for the randomized one with conventional decoder and for the genie decoder. The SINR reduces to:

$$\gamma_k = \| h'_k \|^2 \qquad .....(13)$$

Properties of this equivalent space-frequency channel **˜h** for performance analysis depend on the spatial-temporal dispersion of the multi-path propagation for the MIMO channel H_k, the spatial configuration of the inter-cell interference from the covariance Q_k and the fluctuations of the interference power induced by the multiple access policy (i.e., the variations of Γk), according to the models in the previous sections.

IV. ANALYTICAL PERFORMANCE ASSESSMENT

In this section we derive the performance of the MIMOOFDMA system in terms of the average bit error

probability $\overline{pb} = p_\gamma(\bar{b}_k \neq b_k)$ at the output of the CC. For the sake of clarity, here we focus on BPSK modulation with transmitted symbols $x_k \{\pm 1\}$. Sec. V will extend the analytical methodology to M-QAM modulations. The average bit error probability is evaluated through the union bound as [4].

$$\overline{p_b} \leq \frac{1}{k_{cc}} \sum_{dedfree} \sum_{c \in \varepsilon(d)} \beta(c) P(c)$$

$$= \frac{1}{k_{cc}} \sum_{ded\,free} \sum_{c \in \varepsilon(d)} \beta(c) E_\gamma[P(c \| \gamma)] \quad .....(14)$$

Where d_{free} is the free Hamming distance of the code, $\varepsilon(d)$ is the set of all error events c having Hamming distance d from the all-zero code word, $\beta(c)$ is the input weight and $P(c)$ is the PEP for the error event c. The error probability $P(c)$ is obtained by averaging the conditioned PEP $P(c \| \gamma)$ with respect to using the approach (1). Notice that the d erroneous bits in the error path *c* are mapped onto *d* different subcarriers F = *{f*1, . . . , *fd}* of the data region by the sequence of interleaving, physical-logical subcarrier mapping and scheduling. For every value of d, we need to consider all possible patterns with d erroneous bits in the set $\varepsilon(d)$, as different arrangements of d subcarriers may lead to very different channel correlation values and consequently different error probability values For a given frame, the conditioned PEP $P(c \| \gamma)$ depends on the SINR variants $\gamma = \{\gamma\ 1, \ldots, \gamma d\}$ that are experienced along the subcarriers d, i.e. with instantaneous correlated fading gains H = *{***H**1, . . . ,**Hk***}* and interference configurations $\Gamma = \{\Gamma 1, \ldots, \Gamma k\}$. This probability can be expressed as [4]

$$P(c|\gamma) = P(c|H,\Gamma) = Q\left(\sqrt{2\gamma_{eff}(h,\Gamma)}\right) \quad .....(15)$$

Where the *effective SINR* γ_{eff} (H, Γ) is defined as γ_{eff} (H, Γ) $= \sum_{k \in f} \gamma_k$. To ease the analysis, it is convenient to write the effective SINR as

$$\gamma_{eff}\ (H,\ \Gamma) = \sum_{k \in f} \| h_k \|^2 \quad .....(16)$$

as a function of the *NTNR* × 1 channel vector

$$h = \left[h_{f1}^T, \ldots \ldots \ldots h_{fd}^T\right]^T \quad .....(17)$$

This gathers the channel responses (13) for all subcarriers associated with the error event c.

The average of the conditioned PEP, $E_H[P(c|\gamma)]$, with respect to $\gamma = \gamma(H, \Gamma)$ is derived according to (1), first with respect to the channel *H* for a given pattern Γ and then over the possible interference configurations. In particular, the first average (E_H [.]) is evaluated in Sec. IV-A, taking into account that the SINR variates γ are generally correlated due to the frequency selectivity of multipath channel. Generally speaking, the more error bits are spread in the frequency domain, the lower is the correlation among SINR variates and the higher is the diversity offered by the channel. The second average over the interference patterns (E_H [.]) is discussed in Sec.IV-C.

A. Average over the fading

The average of the conditioned PEP with respect to the fading is

$$P(c|\Gamma) = E_H[P(c|H,\Gamma)]$$

$$= \int Q\left(\sqrt{2\gamma_{eff}}\right) P((\gamma_{eff}|\Gamma)\, d\gamma_{eff}) \quad .....(18)$$

Where we used the compact notation $\gamma_{eff} = \gamma_{eff}$ (H, Γ) for the effective SINR (16) and $P(\gamma_{eff}|\Gamma)$ for its probability density function (pdf). This pdf can be obtained from (16) by using the Rayleigh fading assumption and the correlation properties of $\tilde{\mathbf{h}}$ as described below.

Based on the Rayleigh multi-path fading model, the space time channel is characterized by a spatial-temporal dispersion which directly reflects on the correlation of the space frequency channel response. According to the definition (17), the space-frequency channel (evaluated in the positions related to the error event) can be expressed as $\tilde{\mathbf{h}} \sim \mathcal{CN}(\mathbf{0}, \mathbf{Rd})$ where the covariance matrix is

$$Rd = E[h'_k, h'^H_k]$$

Here $E[h'_k, h'^H_k]$ is the NT*N*R × *NTN*R spatial cross-correlation for the MIMO channel between the hth and kth subcarriers, weighted by the interference contributions *{*Qk,Qh*}* according to (12). Notice that the cross-correlation of the equivalent channel is evaluated in (19) only among the subcarriers selected by the specific

error event c.

According to the channel model in Sec. II-D, the correlation matrix of the multipath channel response is:

$$R_{S,h} = \sum_{\gamma=1}^{W} p_\gamma R_{S,\gamma} G_k G_h \exp\left(-j2\pi \frac{j_k - j_h}{N} \frac{T_\gamma}{T}\right) \quad .....(20)$$

Where the spatial correlation matrix $R_{s,\gamma}$, is given by:

$$R_{S,\gamma} = E[\mathrm{vec}\left[Q_k^{-H/2} A_\gamma\right] \mathrm{vec}\left[Q_k^{-H/2} A_\gamma\right] \wedge T] \quad .....(21)$$

For the evaluation of the pdf of λ_{eff} in (16), we introduce the eigen value decomposition (EVD) of the covariance matrix (19), $Rd = U \wedge U^H$, where $\wedge = \mathrm{diag}\{\lambda 1,....,^{\lambda} \mathrm{dNTNR}\}$ gathers the eigen values and **U** the corresponding eigenvectors. Using the EVD, we can equivalently write the channel vector as $h_k^{'} = Ub$, with $b = CN(0,\wedge)$ representing the projection of the channel onto the orthonormal basis **U**. It follows that the effective SINR,

$$\gamma_{eff} = \| b \|^2 \quad (22)$$

is the sum of *NTN*R independent exponentially distributed random variables with mean values $\{\{\gamma_i\}_{i=1}^{d.NTNR}$. The moment generating function (MGF) of such a sum is [4]:

$$M_{\gamma eff}(s) = \Pi_{i=1}^{d.ntnr} \frac{1}{1-\lambda_{is}} \quad .....(23)$$

Where $\mu = \mathrm{dNTNR}, \lambda = \min_n\{\lambda_n\}$ and the coefficients Ψ_m are obtained recursively, starting from $\Psi_0 = 1$, according to

$$\Psi_m = \frac{1}{m}[\sum_{j=1}^{d.NTNR}(1-\frac{\lambda}{\lambda_j})^i]\psi_{m-i} \quad .....(24)$$

In case all the dNR*N*T eigenvalues are different (the eigenvalues are not assuming identical values, i.e. $\lambda_i \neq \lambda_j$ with $i \neq j$the pdf can be simplified according to [21] as

$$P((\gamma_{eff}|\Gamma)) = \Sigma_{j=1}^{dNTNR} \frac{A_i}{\lambda_j} \exp(-\gamma_{eff}/\lambda_j) \quad .....(25)$$

Where the coefficients A_i are

$$A_i = [\Pi_{i=1}^{d.NTNR} \frac{1}{1-\lambda_{is}}]^T \quad .....(26)$$

Employing (26), we can further approximate (18) adopting the Chernoff bound of the Q-function Q(x) $\leq \frac{1}{2}\exp\left(\frac{-x^2}{2}\right)$ and integrating over the effective SINR. Hence, after straightforward algebraic manipulations, the average PEP can be written as

$$P(c|\Gamma) = \Sigma_{j=1}^{dNTNR} \frac{Ai+1}{\lambda_j} \quad .....(27)$$

B. Codeword bound

To evaluate the bit error probability (14) we have to account for all the possible codeword's of the set $\varepsilon(d)$ for a given d. The cardinality of $\varepsilon(d)$ varies with respect to the specific CC and it usually grows for increasing Hamming distance. Notice also that interleaver and scheduler scramble the bits of each codeword in different ways giving rise to a large number of patterns of subcarriers carrying the unmatched bits. Due to the selectivity of the channel, each configuration experiences a different degree of diversity. For example, let us consider the CC with generator polynomials [171, 133]: at the free distance dfree = 10 the set $\varepsilon(d\,free)$ is composed by 11 possible error paths. Hence the computation of (14) requires the evaluation of at least these 11 configurations.

To avoid the exhaustive computation of all the error events for a given set $\varepsilon(d)$, in the high SINR region we simplify the bound (14) by upper bounding each PEP with the PEP of the code word Cw,d associated to the configuration of d bits that achieves the minimum degree of diversity (or equivalently, the maximum correlation of the SINR values over *f*) at the output of the scrambling process, thus leading to p(c) ≤ *P(*Cw,d). In this way the system performance (14) is further bounded As

$$\overline{pb} = \frac{1}{k_{cc}} \sum_{ded\,free} \beta_d P(Cw,d) \quad .....(28)$$

With $\beta_d = \sum_{c\varepsilon\varepsilon(d)} \beta(c)$ Hence, the worst error event *C*w,d is the one that yields the highest PEP. For the maximization we use the expression (29) for the conditioned PEP, upper-bounded with $\sin^2(\theta) \leq 1$ (see also [37]), i.e.:

$$P(c|\Gamma) \leq \frac{1}{2} \Pi_{i=1}^{dNTNR} \frac{1}{1+\lambda_i} \quad .....(29)$$

C. Average over interference scenarios

In this section we derive the average of the error probability over the possible interference scenarios Γ according to

the two interference management strategies described in Sec. II-B. In case of interference coordinated policy, the interference pattern is constant over the whole data region so that $\Gamma_k = \Gamma$ and $\mathbf{Q}_k = \mathbf{Q}$, thereby, the average over Γ is no needed. On the other hand, in the randomized approach the permutation of the subcarriers makes the interference scenario Γ_k randomly fluctuate along and the average PEP has to account for all the possible levels of interference. According to the assumptions in Sec. III, the overall noise power depends on the number of interferers $v_k = \Gamma_k$ superimposed on the kth subcarrier. The interference power pattern over the error event c can be fully described by the vector of cardinalities $\mathbf{v} = [v_{f1} \ldots\ldots V_{fd}]$. The average of the conditioned PEP can be calculated as

$$P(c) = E_{\Gamma}[P(c|H,\Gamma)] \quad \text{.....(30)}$$

The number of interferers can be considered as a random variable independent from subcarrier to subcarrier, so that

$$\Pr(v) = \Pi_{k=1}^{d} \Pr(v_{fk}) \quad \text{.....(31)}$$

Where each term $\Pr(v_{fk}$ follows the binomial distribution:

$$\Pr(v) = \binom{N_1}{v} \eta^{v} (1-\eta)^{N_1 - 1} \quad \text{.....(32)}$$

The conditioned PEP $P(c \| v)$ is obtained through the equations (18) and (24), or directly (29), by averaging over the effective SINR (16) for a given interference configuration. We recall that each component γ_k of γ_{eff} is defined according to (10) or (11) depending on the interference information available at the receiver (either conventional or ideal genie decoder).

The conventional decoder has knowledge only of the average noise-plus-interference power, thereby, for a given interference pattern, the power $\bar{\sigma}^{-2}$ in (10) is the average over the error event:

$$\bar{\sigma}^{-2} = \frac{1}{d} \sum_{k \in F} \sigma_k^2 \quad \text{.....(33)}$$

Where $V_k = \frac{1}{d} \sum_{k \in F} V_k$ is the average number of active users sharing the same frequencies. The expression (30) simplifies to the average over the values of the scalar variable employing (31) as the probability for a scenario

On the other hand, the ideal case of a genie decoder is based on the instantaneous interference power knowledge (11). In this case the computation of the conditioned PEP has to be performed over each of the possible configuration of **v**. This number is unfeasible for any practical performance assessment. For this reason, in Sec. VI the expectation (30) will be evaluated semi-analytically by Monte-Carlo averaging over a number of random realizations of **v** generated according to the distribution (32).

V. BIT-INTERLEAVED MULTILEVEL PERFORMANCE EVALUATION

In the sequel we extend the performance evaluation to higher order modulations. Without loss of generality, we consider a fixed interference scenario, dropping the symbol Γ in the notation (the average over Γ can be carried out as described in Sec. IV-C). We focus on a MQAM modulation, with modulation set of dimension defining the transmitted symbols as $s_k = \left(s_K^Q + j s_k^I\right)\sqrt{E_g}$ with S_K^Q, $\square\square \in \{\pm 1, \pm 3, \ldots \pm\sqrt{\square} - 1\}$ Where $\square_{\square} = \frac{3}{2(\square - 1)}$ is the transmitted waveform energy. We restrict the analysis to BICM with Max-Log-Map demodulation.

Compared to the error probability derivation in Sec. IV, here the average PEP for an error event c of Hamming distance depends not only on the subcarriers but also on the symbols of the M-QAM constellation and the positions in the *bit* labels that are associated with the erroneous bits. More specifically, let us consider the h bit the interleaver maps such a bit to a constellation symbol on the subcarrier and to a position in the modulation label set. We can express the interleaver effect by writing the sets, $L = \{l1, \ldots l_d\}$ and $\square = \{x1, \ldots, xd\}$, as shown in Fig. 4. We point out that the transmitted symbol $xk \in S$ depends not only on the bit in l_k but also on the remaining m ? 1 bits of the label. They are selected (by the interleaver) from different positions of the same coded block, thus we can consider the other m - 1 bits as independent variables. We further suppose that each bit of the error event is assigned to a different frequency: $f_i \neq f_i$ for $i \neq j$ where $\{i,j\} = 1, \ldots, d$. This is a simplification as an interleaver (acting on a finite length coded sequence) can associate to the same frequency two or more erroneous bits of the same error event. The average PEP can be obtained as [16]:

$$P(c) \leq \Sigma_{\square} \square(\square)\square(\square|\square,\square) \quad .....(34)$$

Where $\square(\square|\square,\square)$ is the PEP conditioned to the set $(\square,\square,)$ while $P(L) = 1/m^{d}$ is the probability of each label set. Notice that for any coded bit sequence to be modulated and any given label set L, there are $2^{(m-1)d}$ possible symbol sequences $\square$ with equal probability $P(\square) = 1/2^{(m-1)d}$

As in the BPSK case, the conditioned PEP $\square(\square|\square,\square)$ depends on the effective SINR $\square$eff that is a linear combination of the SINR values $\square\square = \{\square\square 1, \ldots, \square\square\square\}$. Here, however, each SINR value $\square\square$ has to be scaled by a factor to account for the Euclidean distance between the transmitted symbol and its nearest concurrent in the considered symbol constellation, hereinafter denoted as $\Delta^2 k$.This factor can vary with x_k and l_k. More specifically, for a QAM modulation, let S_0^l and S_1^l) be the subset of all symbols x_k whose label has the value 0 (and 1) in position l_k , for l_k = 1. . . (see [16]). Fig. 4 shows the subset $S2^1$ focusing on the d_{th} bit of the received code word, accounting for M=16 with Gray's mapping. If the transmitted bit is equal to 1 and it is mapped onto the *l*th label position, the transmitted symbol x_k belongs to the subset S_1^1 . The Max-Log-Map demodulator decision is erroneous when the received symbol lies in S_0^1. Thereby, the probability of error can be upper bounded by using the Euclidean distance between x_k and the boundary of the area associated to the nearest neighbor in S_0^1. For the 16-QAM example in Fig. 4 ($I_d = 2$), this distance is $\sqrt{\square_{\square}}\Delta_{\square}$, with Δ_k = 1 for ever

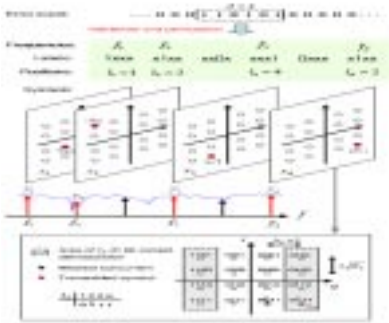

Fig. 4. Example of interleaver assignment of an error event (for all-zeros transmitted sequences)

considering a 16QAM modulation. The *k*th coded bit is mapped over the frequency in the QAM symbol and in the label position. The plot below shows the areas of correct decision for the kth bit.

Symbols x_k , therefore this value does not depend on the other *m* - 1 bits. The same holds for label position *l* = 4. On the other hand, for label positions *l* = 1 and *l* = 3 the value of the scaled distance is $\Delta_k = 1$ for half symbols and $\Delta_k = 2$ for the other half symbols. It follows that the k_{th} bit experiences the SINR:

$$\square_{\square} = \frac{\square_0}{\square_{\square}} \frac{3}{2(\square^2 - 1)} \Delta_{\square}^2 \| \dot{\square}_{\square} \|^2 \quad .....(35)$$

The modified expression is used to rewrite the effective SINR (16) as a function of the set of *??* Euclidean distances $\{\Delta_1, ..., \Delta_k\}$

Thereby the corresponding PEP becomes:

$$\square(\square|\square,\square) = \square(\square|\square) = \square_{\square}[\square(\sqrt{2\square_{\text{eff}}(\gamma,D)})] \quad .....(36)$$

It is worth noticing that each distance Δ_k can assume only few values. As a matter of fact, for the 16-QAM constellation in Fig. 4 it is $\Delta_k = 1$ for three quarters of the sets and $\Delta_k = 3$ for the remainder, i.e.: $(\Delta_k = 1) = 3/4$ and $(\Delta_k = 3) = 1/4$ .Similar considerations holds for 64-QAM whereas it can be easily observed that for QPSK (n = 4) it is $\Delta_k = 1$ and the effective SINR simplified. For BPSK modulation it is $\Delta_k = 1/2$ .Since only few distance values are observed, it is convenient to gather in (38) all the configurations that correspond to the same distance set c, yielding:

$$P(c) = \square_{\square}[\square(\square|\square_I)] \quad .....(37)$$

Where (p(D)) is the probability of the distance set *c*. However, in order to avoid the expensive EVD for each configuration of we propose to approximate the expectation by means of a sample average: we simulate some values as the outcomes of i.i.d. random variables, having known distribution (see the probabilities above for 16-QAM); for each value, the effective SINR is obtained and its pdf is calculated according to the approach in Sec. IV-A; the estimate of the average bit error probability is then obtained by averaging over some realizations.

VI. PERFORMANCE ANALYSIS

This section gives the performance evaluation of the proposed method under various regards.

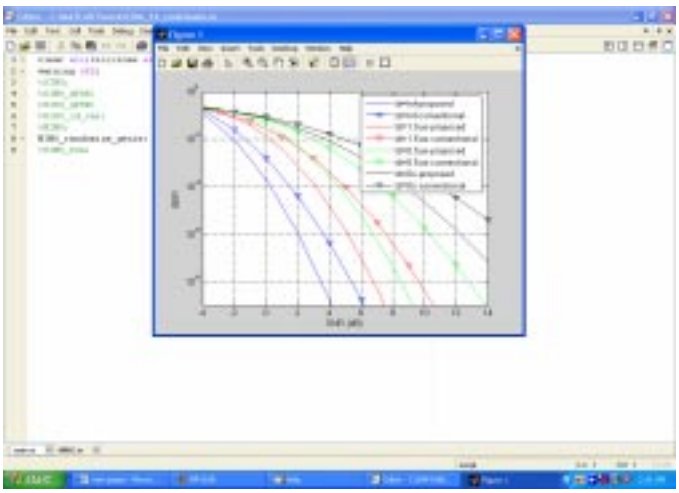

Fig5 : *Performance of the proposed method at various Doppler frequencies*

The above figure represents the Bit error rate versus Signal to noise ratio plot. From the above figure it is clear that the performance of the proposed method for various Doppler affects (1ns, 1.5us,.5us,0us) is efficient. It also denotes that with an increase in SNR value at there is a nominal decrease in the BER of the proposed method is decreasing due to the availability of multiple channels, thus the total SINR is going to be decreased. Thus this decreased value provides the optimum power allocation for users.

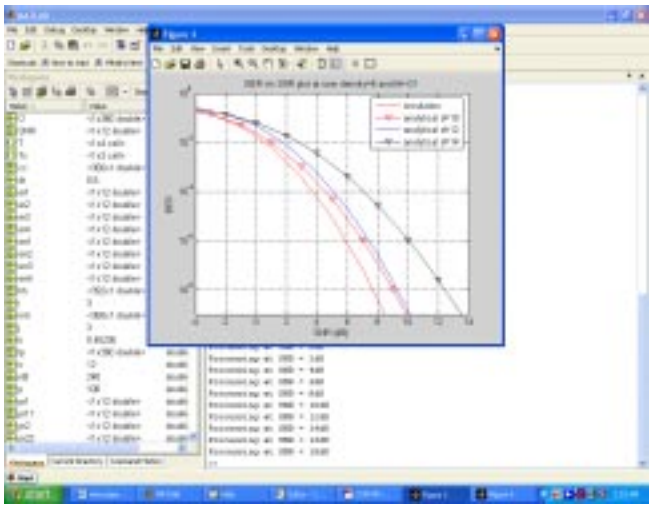

Fig.6 Analytic and simulated BER vs traffic load in randomized interference scenario with ideal genie decoder. Performance of a SISO IEEE 802.16-e system with QPSK, convolutional code WiMAXcc1, Interference randomization with PUSC strategy and fixed delay spread = 1s.

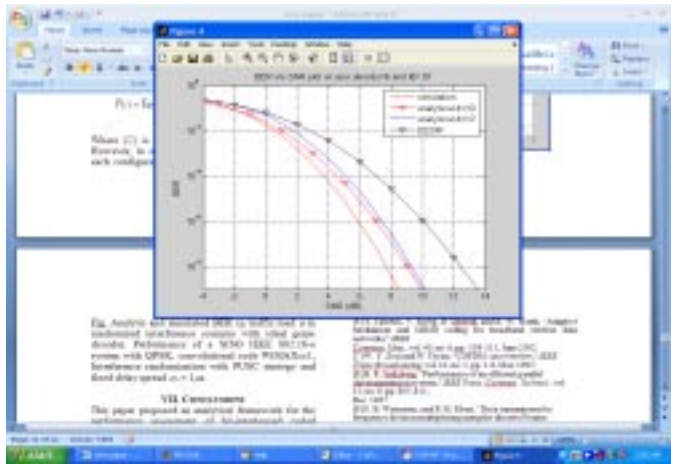

Fig.7 BER vs SINR in coordinated interference scenario with 3GPP SCM Model III for the proposed analytical bound and the EESM method. SIMO IEEE 802.16-d system with QPSK, convolutional code WiMAXcc1, interference cancellation with MVDR filtering and full traffic load.

The above Fig. shows the comparison between the two methods for the IEEE 802.16-d beam forming scenario with QPSK modulation and code WiMAXcc1. Conclusions are described in next section

VII. CONCLUSIONS

This paper proposed an analytical framework for the performance assessment of bit-interleaved coded multi-antenna OFDMA systems over space-frequency selective fading channels with application to practical 4G broadband wireless standards. Since the analysis is fairly complex due to the wide spectrum of system configurations and channel/interference scenarios, some assumptions have been made to narrow the applications. A multicell scenario has been considered for inter-cell interference based on either coordinated or randomized multi-user access. The analytical formulation accounts for the spatial-frequency selectivity of the fading channel and possible non-stationary interference due to subcarrier randomization. Both beamforming and diversity schemes have been considered as multi-antenna systems. The analysis has been carried out for convolutionally coded BICM systems with BPSK modulation, and then extended to higher order modulations. Two practical standards have been used as benchmark for the analytical analysis, 3GPP LTEand WiMAX IEEE 802.16d-e . Simulation results proved the validity of the analysis for a wide range of system configurations, propagation scenarios, interference conditions and system

loads. Finally, the proposed methodology shows high accuracy with huge computational cost reduction with respect to common link level simulations.

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A Novel Nash Equilibrium Technique for Channel Allocation in Multihop Wireless Networks

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ABSTRACT

This Paper Presents, a Novel technique for fixed channel allocation using Na Equilibrium process in Multihop Wireless Networks. A hierarchical strategy is followed for channel allocation to involve both cooperative and non cooperative to gain the best date data rates throughout the communication in wireless network. This Algorithm uses Min-Max Coalition-Proof Nash Equilibrium to achieve the good data rate in all sessions. The fundamental process of an algorithm, simulation results and limitations are discussed.

Index Terms

Multihop wireless Networks, Nash equilibrium, Multiple radio, Game theory etc.

1. Introduction

Cellular communications become increasingly popular and mobile subscribers are expected to rise heavily. Besides cellular communications, Ad hoc networking is another type of wireless communication technology. Traditional cellular networks and mobile ad hoc networks both have their respective advantages and drawbacks. Traditional cellular networks have mature technology support for reliable performance. However, building and expanding their necessary infrastructure is costly. Multihop wireless networks, on the other hand, are simple to deploy and easily expandable. In wireless communication the wireless medium is shared by the different user through the multiple access techniques. The total available bandwidth is divided permanently into a number of distinct sub bands named as channels. Commonly, we refer to the assignment of radio transceivers to these channels as the channel allocation problem.

In this paper, we present a game-theoretic analysis of fixed channel allocation strategies of devices that use multiple radios in the multihop wireless networks. Static non cooperative game is a novel approach to solve the channel allocation problem in single-hop networks, and Nash equilibrium (NE) provides an efficient criterion to evaluate a given channel allocation. In multihop networks, however, noncooperative game results in low achieved data rate for multihop sessions and low throughput for whole networks due to the reasons mentioned in Section 4. Hence, we introduce a hybrid game involving both cooperative game and noncooperative game into our system in which the players within a communication session are cooperative, and among sessions, they are noncooperative.

Multihop wireless Networks

A multi-hop wireless network is characterized by the absence of a direct communication link between source and destination nodes. Data transmission in this case must first be transmitted to nearby relay nodes, which in turn forward data to the destination node. This class of networks has a wide range of applications such as wireless ad hoc networks, wireless mesh networks, wireless sensor networks, and multi-hop cellular networks. A multi-hop wireless network enables short-range communication while preserving broad service coverage. Short-range communications leads to higher received SINR. Therefore, transmitting power can be reduced without compromising packet error probability. The reduction in power requirement

implies longer battery lifetime, and smaller interfering region which could result in an increase in spatial reuse. Alternatively, with fixed transmission power, short-range communications leads to decreased packet error probability, hence allowing higher modulation order transmission which is more susceptible to noise.

Short-range communication not only improves aver- age throughput, but also helps distribute services fairly among mobiles with poorer channel condition. An example of multi-hop wireless networks is illustrated in fig. 2, where Mobiles 1 and 2 are close to the base station, and therefore their SINR levels are expected to be comparatively high. Mobile 3, on the other hand, is far from the base station and obstructed by a building, and therefore the link between Mobile 3 and the base station experiences high path loss and shadowing, leading to low SINR. Although increasing transmitting power can solve this problem, it might lead to more interference and inefficient energy usage. Another solution is to transmit data to Mobile 3 via a relay node. Transmission in a multi-hop manner could Lead to better throughput.

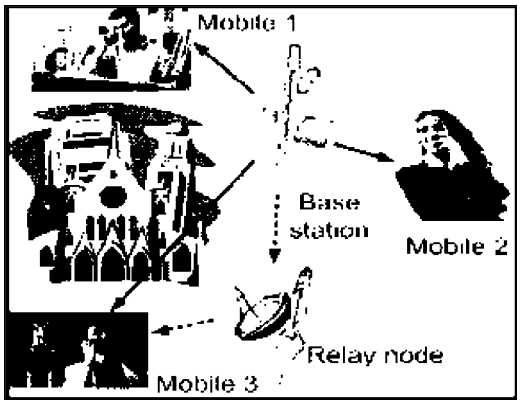


Fig. 1: *A Multihop Cellular Network*

Due to the lack of any central controller, problems in a multi-hop wireless network are generally more challenging than those in a cellular wireless network. In a multi- hop wireless network, each mobile coordinates with each other to keep the network up and running. Scheduling could be difficult, since most algorithms for multi-hop networks are usually in a distributed manner. Error control on the other hand could be conducted in the same way as it is in a cellular wireless network. For a multi-hop wireless network, this dissertation models and analyzes the impact of a class of ARQ protocols on the performance of in a multi-hop wireless data network. The analysis is divided into two parts. The first part models the number of transmissions for successful delivery of a packet across a multi-hop path. The second part studies the performance of batch transmission in a multi-hop wireless network only with a small number of hops. The novelty of these models is that the probability mass function (pmf) for the number of transmissions required for end-to-end delivery of a packet or a batch of packets can be obtained under different hop-level error control policies. Therefore, the trade-off between reliability and latency can be analyzed. Scheduling is one of the most important components of radio link design for cellular wireless networks. In the literature, it was shown that a channel-qualitybased opportunistic scheduling can be used to maximize resource usage (system throughput). However, the impact of Adaptive

Modulation and Coding (AMC), ARQ, and channel variation on this scheduling algorithm was not thoroughly investigated. This work derives complete statistics (i.e., probability density function (pdf)/probability mass function (pmf)) for the delay and throughput of this type of scheduling. The statistics can be used to adjust the network parameters such as the level of Quality of Service (QoS), radio link layer parameter settings, and the number of admissible connections so that the radio link performance can be optimized. Another type of scheduling, namely, fair scheduling aims at allocating resources among customers in proportion to their weights. This type of scheduling algorithm would be useful to classify customers based on their levels of subscription. For example, premium-class customers should acquire larger portions of service than regular- class customers. This dissertation proposes two fair scheduling algorithms for cellular networks under single-rate and multi-rate transmissions. Both algorithms show improved performance over the algorithms in the literature. As cellular networks evolve towards the next-generation wireless networks, in- corporation of multi-hop communications into the cellular network seems to be in-evitable. This dissertation presents two performance analysis models for multi-hop packet transmissions which reveal the trade-o between latency and reliability under different error control (i.e., retransmission) policies. In particular, ARQ with higher level of persistence provides higher reliability at the expenses of increased latency. For real-time traffic, data packets might become useless after some time. Therefore, the use of infinite-persistence ARQ may not be appropriate. The analytical model would be useful for engineering the network for provisioning required QoS for the different types of service in a multi-hop wireless setup.

The rest of the paper is organized as follows: Section 2 represents the previous work of channel allocation schemes. In Section 3 the system design is discussed. In section 4 the hierarchical steps of a Nash equilibrium algorithm is discussed in detail and in Section 5 presents the simulation results. Finally conclusion is made in Section 6.

2. Related Work

There has been a considerable amount of research on channel allocation in wireless networks, especially in cellular networks. Three major categories of channel allocation schemes are always used in cellular networks: fixed channel allocation (FCA), dynamic channel allocation (DCA), and hybrid channel allocation (HCA) which is a combination of both FCA and DCA techniques.

In FCA schemes, a set of channels is permanently allocated to each cell in the network. In general, graph coloring/labeling technique provides an efficient way to solve the problems of fixed channel allocation. FCA method can achieve satisfactory performance under a heavy traffic load; however, it cannot adapt to the change of traffic conditions or user distributions. To overcome the inflexibility of FCA, many researchers propose dynamic channel allocation methods. In DCA schemes, in contrast, there is no constant relationship between the cells and their respective channels. All channels are potentially available to all cells and are assigned dynamically to cells as new calls arrive in. Because of its dynamic property, the DCA method can adapt to the change of traffic demand. However, when the traffic load is heavy, DCA method performs worse than FCA due to some cost brought by adaptation.

Hybrid channel allocation schemes are the combination of both FCA and DCA techniques. In HCA schemes, the total number of available channels are divided into fixed and dynamic sets. The fixed set contains a number of nominal channels that are assigned to the cells as in the FCA schemes, whereas the dynamic set is shared by all users in the system to increase flexibility.

Recently, channel allocation problem is becoming a focus of research again due to the appearance of new communication technologies, e.g., wireless local area networks (WLANs), wireless mesh networks (WMNs).

In WMNs, many researchers have considered devices using multiple radios. Equipping multiple with radios in the devices in WMNs, especially the devices acting as wireless routers, can improve the capacity by transmitting over multiple radios simultaneously using orthogonal channels. In the multiradio communication context, channel allocation and access are also considered as the vital topics. By joint considering the channel assignment and routing problem, Alicherry et al. propose an algorithm to optimize the overall throughput of WMNs.

In the above cited work, the authors make the assumption that the devices cooperate with the purpose of the achievement of high system performance. However, this assumption might not hold for the following two reasons. In one hand, players are usually selfish who would like to maximize their own performance without considering the other players' objective. In the other hand, the full cooperation of arbitrary devices is difficult to achieve due to the transmission distance limitation and transmission interference of neighboring devices. Game theory provides a straightforward tool to study channel allocation problems in competitive wireless networks. An example of three communication sessions is shown in figure 2.

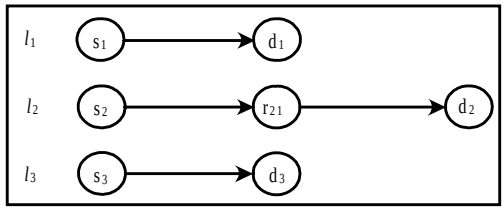


Fig. 2 : *An example of three communications session*

3. System Design

In this paper, we present a game-theoretic analysis of fixed channel allocation strategies of devices that use multiple radios in the multihop wireless networks. Static non cooperative game is a novel approach to solve the channel allocation problem in single-hop networks, and Nash Equilibrium (NE) provides an efficient criterion to evaluate a given channel allocation. In multihop networks, however, noncooperative game results in low achieved data rate for multihop sessions and low throughput for whole networks due to the reasons Hence, we introduce a hybrid game involving both cooperative game and noncooperative game into our system in which the players within a communication session are cooperative, and among sessions, they are noncooperative.

We first define the Min-Max Coalition-Proof Nash Equilibrium (MMCPNE) in this hybrid game, which is aiming to achieve the maximal data rate of all sessions (including single-hop sessions and multihop sessions). We also define three other equilibria schemes that approximate to MMCPNE, named as Minimal Coalition-Proof Nash Equilibrium (MCPNE), Average Coalition-Proof Nash Equilibrium (ACPNE), and I Coalition-Proof Nash Equilibrium (ICPNE), respectively.

Then, we study the existence of MMCPNE in this game and our main result, Theorem 2, shows the necessary conditions for the existence of MMCPNE. Furthermore, we propose the MMCP algorithm which enables the selfish players to converge to MMCPNE from an arbitrary initial configuration and the DCP-x algorithms which enable the players converge to approximated MMCPNE states (e.g., MCPNE, ACPNE, and ICPNE). Finally, we present the simulation results of the proposed algorithms, which show

that MMCPNE outperforms NE and Coalition-Proof Nash Equilibrium (CPNE) channel allocation schemes in terms of the achieved data rates of multihop sessions and the throughput of whole networks due to cooperative gain.

4. Nash Equilibria

A. Noncooperative Game NE

In single-hop networks, the payoff of player i is equivalent to its utility Ri and the multiradio channel allocation problem can be formulated as a static noncooperative game. In order to study the strategic interaction of the players in such a game, we first introduce the concepts of Nash equilibrium.

B. Cooperative Game CPNE

It is worth noting that noncooperative game is not suitable for multihop networks due to the following two reasons. On one hand, the payoff of any player in multihop session is not equivalent to its utility. In fact, the payoff (achieved data rate) of player i is not only determined by the utility itself, but also by the utilities of other players within the same session. On the other hand, it is possible that the players in the same session cooperatively choose their strategies for the purpose of high payoff. Hence, we formulate the problem in multihop networks as a hybrid game involving both cooperative game and noncooperative game. In detail, the players within a coalition (session) are cooperative, and among coalitions, they are noncooperative. In order to study the strategic interaction of the coalitions in cooperative game, we introduce the concept of classical coalition-proof Nash equilibrium

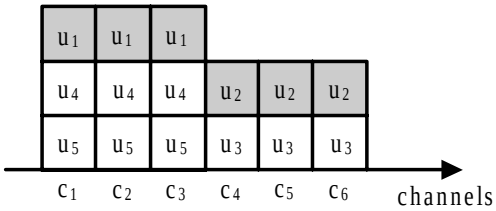
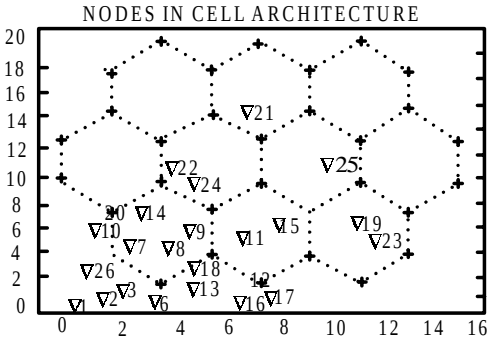
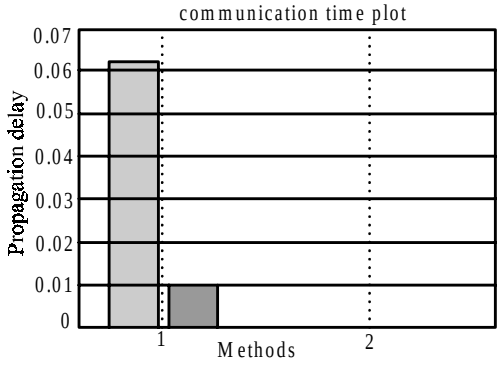
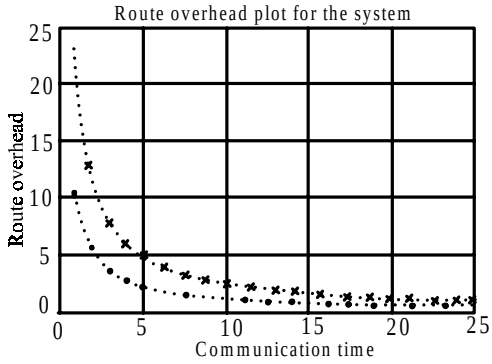


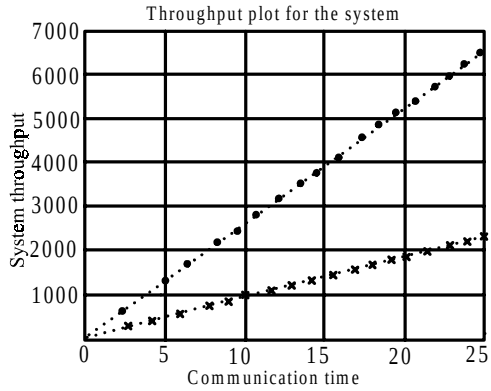
Fig. 3: *An example of CPNE Channel Allocation*

5. Simulation Results









6. Conclusion

Wireless communication system is often assigned a certain range of communication medium (e.g., frequency and). Usually, this medium is shared by different users through multiple access techniques. Frequency Division Multiple Access (FDMA), which enables more than one users to share a given frequency band, is one of the extensively used techniques in wireless networks In order to meet the demands of multi-rate multimedia communications, next generation cellular systems must employ advanced algorithms and techniques that not only increase the data rate, but also enable the system to guarantee the quality of service (QoS) desired by the various media classes. In this work we have investigated a novel approach called nash equilibrium for channel estimation and proper communication between nodes in different topologies

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A Fault Exposure and Data Resurgence EDDR Architecutre for Video Coding Systems

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ABSTRACT

Given the critical role of motion estimation (ME) in a video coder, testing such module is of priority concern. While focusing on the testing of ME in a video coding system, this work presents an error detection and data recovery (EDDR) design, based on the residue-and-quotient (RQ) code, to embed into ME for video coding testing applications. An error in processing elements (PEs), i.e. key components of a ME, can be detected and recovered effectively by using the proposed EDDR design. Experimental results indicate that the proposed EDDR design for ME testing can detect errors and recover data with an acceptable area overhead and timing penalty. Importantly, the proposed EDDR design performs satisfactorily in terms of throughput and reliability for ME testing applications.

Index Terms

Area overhead, data recovery, error detection, motion estimation, reliability, residue-and-quotient (RQ) code.

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INTRODUCTION

Advances in semiconductors, digital signal processing, and communication technologies have made multimedia applications more flexible and reliable. A good example is the H.264 video standard, also known as MPEG-4 Part 10 Advanced Video Coding, which is widely regarded as the next generation video compression standard. Video compression is necessary in a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding systems, a ME is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. Additionally, while performing up to 60%-90% of the computations encountered in the entire coding system, a ME is widely regarded as the most computationally intensive of a video coding system .

A ME generally consists of PEs with a size of 4 x4. However, accelerating the computation speed depends on a large PE array, especially in high-resolution devices with a large search range such as HDTV. Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME. Moreover, although the advance of VLSI technologies facilitate the integration of a large number of PEs of a ME into a chip, the logic-per-pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing on the chip. As a commercial chip, it is absolutely necessary for the ME to introduce design for testability (DFT). DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods rely on reconfiguration of a circuit under test (CUT) to improve testability. While DFT approaches enhance the testability of circuits, advances in sub-micron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world. BIST for the ME does not expensive test equipment, ultimately lowering test costs]. Moreover, BIST can generate test simulations and analyse test responses without outside support, subsequently streamlining the testing and diagnosis of digital systems. However, increasingly complex density of circurity requires that the built in testing approach not only detect faults but also specify their locations for error correcting. Thus, extended schemes of BIST referred to as built-in self-diagnosis and built-in self-correction have been developed recently.

While the extended BIST schemes generally focus on memory circuit, testing-related issues of video coding have seldom been addressed. Thus, exploring the feasibility of an embedded testing approach to detect errors and recover data of a ME is of worthwhile interest. Additionally, the reliability issue of numerous PEs in a ME

can be improved by enhancing the capabilities of concurrent error detection (CED). The CED approach can detect errors through conflicting and undesired results generated from operations on the same operands. CED can also test the circuit at full operating speed without interrupting a system. Thus, based on the CED concept, this work develops a novel EDDR architecture based on the RQ code to detect errors and recovery data in PEs of a ME and, in doing so, further guarantee the excellent reliability for video coding testing applications. The rest of this paper is organized as follows. Section II describes the mathematical model of RQ code and the corresponding circuit design of the RQ code generator (RQCG). Section III then introduces the proposed EDDR architecture, fault model definition, and test method. Next, Section IV evaluates the performance in area overhead, timing penalty, throughput and reliability analysis to demonstrate the feasibility of the proposed EDDR architecture for ME testing applications. Conclusions are finally drawn in Section V.

II. RQ CODE GENERATION

Coding approaches such as parity code, Berger code, and residue code have been considered for design applications to detect circuit errors. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. For instance, assume that N denotes an integer N_1 and N_2 represent data words, and m refers to the modulus. A separate residue code of interest is one in which N is coded as a pair $(N,|N|_m)$. Notably $|N|_m$ is the residue of N modulo m. Error detection logic for operations is typically derived using a separate residue code such that detection logic is simply and easily implemented. However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. Therefore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors. The mathematical model of RQ code is simply described as follows. Assume that binary data X is expressed as

$$X=\{b_{n-1}b_{n-2}.....b_2b_1b_0\}=\sum_{j=0}^{n-1}b_j2^j \qquad .....(1)$$

The RQ code of X modulo m expressed as $R=|X|_m\ Q=[X/m]$, respectively. Notably, $[i]$ denotes the largest integer not exceeding i.

According to the above RQ code expression, the corresponding circuit design of the RQCG can be realized. Inorder to simplify the complexity of circuit design, the implemen- tation of the module is generally dependent on the addition operation. Additionally, based on the concept of residue code, the following definitions shown can be applied to generate the RQ code for circuit design.

Definition 1

$$|N_1+N_2|_m=\left||N_1|_m+|N_2|_m\right|_m \qquad .....(2)$$

Definition 2: Let $N_j=n_1+n_2+..\ +n_j$, then

$$N_j|_m=\|n_1\|_m+|n_2|_m+..\ +\left|n_j|_m\right|_m \qquad .....(3)$$

To accelerate the circuit design of RQCG, the binary data shown in (1) can generally be divided into two parts:

$$X=\sum_{j=0}^{n-1}b_j2^j=\left(\sum_{j=0}^{k-1}b_j2^j\right)+\left(\sum_{j=k}^{n-1}b_j2^{jk}\right)2^k=Y_D+Y_12^k \qquad .....(4)$$

Significantly, the value of k is equal to [n/2] and the data formation of Y_0 and Y_1 are a decimal system. If the modulus $m=2^k-1$, then the residue code of X modulo m is given by

$$R=|X|_m=|Y_0+Y_1|_m=|Z_o+Z_1|_m=(Z_0+Z_1)\alpha$$

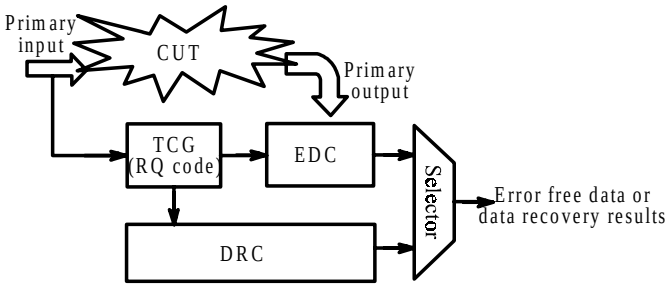


Fig. 1 : *Conceptual view of the proposed EDDR architecture.*

$$Q=\left|\frac{X}{m}\right|=\left[\frac{Y_0+Y_1}{m}\right]+Y_1=\left[\frac{Z_0+Z_1}{m}\right]+Z_1+Y_1$$
$$=Z_1+Y_1+\beta$$

Where

$$Q(\beta)=\begin{cases}0(1), & \text{if } Z_0+Z_1=m\\ 1(0), & \text{if } Z_0+Z_1<m\end{cases}$$

Notably, since the value of Y_0+Y_1 is generally greater than that of modulus m, the equations in (5) and (6) must be simplified further to replace the complex module operation with a simple addition operation by using the parameters Z_0, Z_1, Q and β.

Based on (5) and (6), the corresponding circuit design of the RQCG is easily realized by using the simple adders (ADDs). Namely, the RQ code can be generated with a low complexity and little hardware cost.

III. PROPOSED EDDR ARCHITECTURE DESIGN

Fig. 1 shows the conceptual view of the proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in Fig. 1 utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data.

This work adopts the systolic ME [19] as a CUT to demonstrate the feasibility of the proposed EDDR architecture. A ME consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. A PE generally consists of two ADDs (i.e. an 8-b ADD and a 12-b ADD) and an accumulator (ACC). Next, the 8-b ADD (a pixel has 8-b data) is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications [20]. Notably, some registers and latched may exist in ME to complete the data shift and storage.

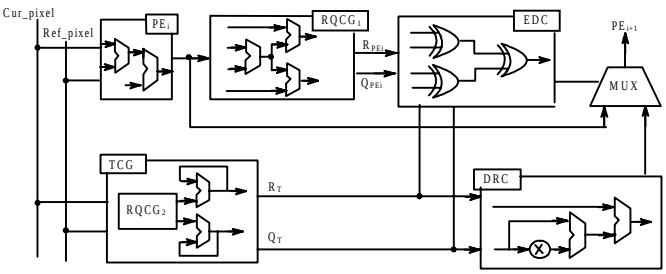


Fig. 2 : *A specific testing processes of the proposed EDDR architecture.*

Fig. 2 shows an example of the proposed EDDR circuit design for a specific of a ME. The fault model definition, RQCG-based TCG design, operations of error detection and data recovery, and the overall test strategy are described carefully as follows.

A. Fault Model

The PEs are essential building blocks and are connected regularly to construct a ME. Generally, PEs are surrounded by sets of ADDs and accumulators that determine how data flows through them. PEs can thus be considered the class of circuits called ILAs, whose testing assignment can be easily achieved by using the fault model, cell fault model (CFM) [21]. Using CFM has received considerable interest due to accelerated growth in the use of high-level synthesis, as well as the parallel increase in complexity and density of integration circuits (ICs). Using CFM makes the tests independent of the adopted synthesis tool and vendor library. Arithmetic modules, like ADDs (the primary element in a PE), due to their regularity, are designed in an extremely dense configuration.

Moreover, a more comprehensive fault model, i.e. the stuck-at (SA) model, must be adopted to cover actual failures in the interconnect data bus between PEs [22]. The SA fault is a well- known structural fault model, which assumes that faults cause a line in the circuit to behave as if it were permanently at logic "0" (stuck-at 0 (SA0)) or logic "1" [stuck-at 1 (SA1)]. The SA fault in a ME architecture can incur errors in computing SAD values. A distorted computational error and the magnitude of are assumed here to be equal to $SAD'–SAD$, where SAD' denotes the computed SAD value with SA faults.

B. TCG Design

According to Fig. 2, TCG is an important component of the proposed EDDR architecture. Notably, TCG design is based on the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data. The specific PE_i in Fig. 2 estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macroblock. Thus, by utilizing PEs, SAD shown in as follows, in a macroblock with size of N x N can be evaluated:

$$SAD = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}\left|X_{ij} - Y_{ij}\right| = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}\left|\left(q_{xij}.m + r_{xij}\right) - \left(q_{yij}.m + r_{yij}\right)\right| \quad .....(7)$$

where $r_{xij}q_{xij}$ and $r_{yij}q_{yij}$ denotes the corresponding RQ code of X_{ij} and Y_{ij} modulo m. Importantly, X_{ij} and Y_{ij} represent the luminance of Cur_pixel and Ref_pixel, respectively. Based on the residue code, the definitions shown in (2) and (3) can be applied to facilitate

generation of the RQ code pixel value $(R_T \text{ and } Q_T)$ form TCG. Namely, the circuit design of TCG can be easily achieved (see Fig. 3) by using

$$R_T = \left|\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij} - Y_{ij})\right|_m$$

$$= \left\|(X_{00} - Y_{00})\right|_m + \left|(X_{01} - Y_{01})\right|_m + ... + \left|(X_{[N1](N1)}Y_{[N1](N1)})\right|_m\Big|_m$$

$$= \left\|(q_{x00}.m + r_{x00})(q_{y00}.m + r_{y00})\right|_m + ...$$

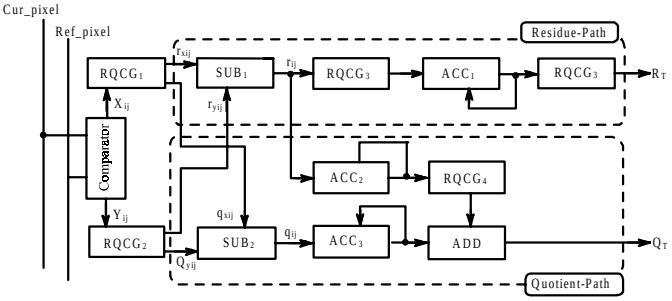
$$.\left|(q_{x(N1)(N1)}.m + r_{x(N1)(N1)})(q_{b(N1)[N1]}.m + r_{y(N1)(N1)})\right|_m\Big|_m$$

$$= \left\|\left|(r_{x00}\ r_{y00})\right|_m + (r_{x01}\ r_{y00})\right|_m + (r_{x01}\ r_{y01})\Big|_m + ...$$

$$(r_{x(N1)(N1)}\ r_{x(N1)(N1)})\Big|_m\Big|_m - \left\|r_{00}\right|_m + \left|r_{01}\right|_m + ... + \left|r_{(N-1)(N-1)}\right|_m\Big|_m$$

(8) and (9), shown at the bottom of the following page, to derive the corresponding RQ code.

Fig. 4 shows the timing chart for a macroblock with a size of 4 x4 in a specific FE_i demonstrate the operations of the TCG circuit. The data n_0 and n_1 from Cur_pixel and Ref_pixedl must be sent to a comparator in order to determine the luminance pixel value X_{ij} and Y_{ij} at the 1st clock. Notably, if $X_{ij} \geq Y_{ij}$., then X_{ij} and Y_{ij} are the luminance pixel value of Cur_pixel Fig. 3. Circuit design of the TCG and Ref_pixel, respectively. Conversely, X_{ij} represents the luinance pixel value of Ref_pixel, and Y_{ij} denotes the luminance pixel value of Cur_pixel when $X_{ij} < Y_{ij}$ At the 2nd clock, the values of X_{00} and Y_{00} are generated and the corresponding RQ code r_{x00}, q_{x00}, r_{y00}, q_{y00} can be captured by the $RQCG_1$ and $RQCG_2$ circuits if the 3rd clock is triggered.



Equations (8) and (9) clearly indicate that the codes of r_{00} and q_{00} can be obtained by using the circuit of a subtracter (SUB). The 4th clock displays the operating results. The modulus value of r_{00} is then obtained at the 5th clock. Next, the summation of quotient values and residue values of modulo are proceeded with from clocks 5-21 through the circuits of ACCs. Since a 4 macroblock in a specific FE_i pixels of a ME contains 16, the corresponding RQ code $(R_T \text{ and } Q_T)$ is exported to the EDC and DRC circuits in order to detect errors and recover data after 22 clocks. Based on the TCG circuit design shown in Fig. 4, the error detection and data recovery operations of a specific FE_i in a ME can be achieved.

C. EDDR Processes

Fig. 2 clearly indicates that the operations of error detection in a specific pE_i is achieved by using EDC, which is utilized to compare the outputs between TCG and $RQCG_1$ in order to determine whether errors have occurred. If the values of $R_{PFi} \neq R_T$ and/or $Q_{PF_i} \neq Q_T$ then the errors in a specific PE_i can be detected. The EDC output is then used to generate a 0/1 signal to indicate that the tested PE_i is error-free/errancy.

This work presents a mathematical statement to verify the operations of error detection. Based on the definition of the fault model, the SAD value is influenced if either SA1 and/or SA0 errors have occurred in a specific PE_i. In other words, the SAD value is transformed to $SAD' = SAD + e$ if an error occurred. Notably, the error signal is expressed as

$$\in = q_n.m + r_n \qquad .....(10)$$

to comply with the definition of RQ code. Under the faulty case the RQ code from $RQCG_2$ of the TCG is still equal to (8) and 9). However, R_{PE_i} and Q_{PE_i} are changed to (13) and (14) because an error has occurred. Thus, the error in a specific PE_i can be detected if and only if (8) ≠ (11) and/or (9) ≠ (12)

$$R_{PE_i} = \left|SAD'\right|_m$$

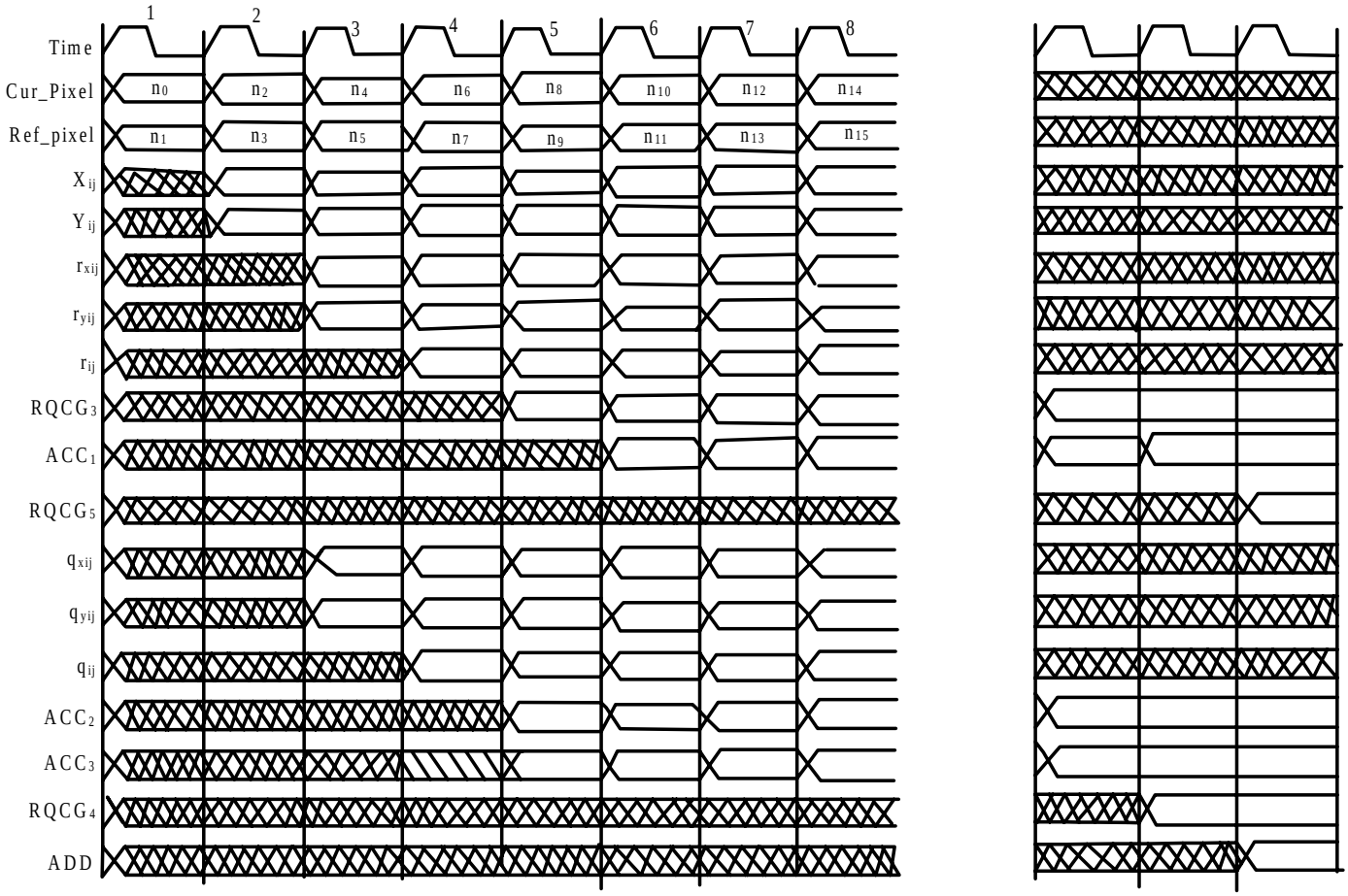
$$Q_T = \left\lfloor \frac{\sum_{i-0}^{N\,1\,N\,1}\sum_{j-0}(X_{ij}\ \ y_{ij}}{m} \right\rfloor$$

$$\left\lfloor \frac{(X_{00}\ \ Y_{00}) + (X_{01}\ \ Y_{01}) + ... + (X_{(N-1)(N-1)}\ \ (Y_{(N-1)(N-1)})}{m} \right\rfloor$$

$$\left\lfloor \frac{(q_{x00}.m - q_{y00}.m)}{m} + \frac{(r_{x00} - r_{y00})}{m} + \frac{(q_{x01}.m - q_{y01}.m)}{m} + \frac{(r_{x01} - r_{y01})}{m} + \ldots \right\rfloor$$

$$= \left\lfloor (q_{x00}\ \ q_{y00}) + (q_{x01}\ \ q_{y01}) + \ldots\ldots + \frac{(r_{x00} - r_{y00}) + (r_{x01} - r_{y01}) + \ldots}{m}. \right\rfloor$$

$$= q_{00} + q_{01} + \ldots + q(N \quad 1)(N \quad 1) + \left\lfloor \frac{(r_{oo} + r_{01} + \ldots . r_{(N-1)(N-1)})}{m} \right\rfloor$$



$$\left| \sum_{i-0}^{N\ 1} \sum_{j-0}^{N\ 1} (X_{ij}\ \ y_{ij}) + e \right|_m$$

$$\left| r_{00} \right|_m + \left| r_{01} \right|_m + \ldots + \left| r_{(N-1)(N-1)} \right|_m \quad + \left| r_e \right\| m \left|_m \right.$$

$$Q_{PE_i} = \left\lfloor \frac{SAD'}{m} \right\rfloor$$

$$\left\lfloor \frac{\sum_{i-0}^{N\ 1} \sum_{j-0}^{N\ 1} (X_{ij}\ \ y_{ij}) + e}{m} \right\rfloor$$

$$q_{00} + q_{01} + \ldots q_{(N \quad 1)(N \quad 1)} + q_e + \left\lfloor \frac{(r_{00} + r_{01} + \ldots r_{(N-1)(N-1)} + r_e}{m} \right\rfloor$$

During data recovery, the circuit DRC plays a significant role in recovering RQ code from TCG. The data can be recovered by implementing the mathematical model as

$$SAD = m \times Q_r + R_T$$
$$= (2^j - 1) \times Q_T + R_T$$
$$= 2^j \times Q_T \quad Q_T + R_T \qquad (13)$$

To realize the operation of data recovery in (13), a Barrel shift [23] and a corrector circuits are necessary to achieve the functions of $(2^j \times Q_T)$ and $(-Q_T + R_T)$ respectively. Notably, the proposed EDDR design executes the error detection and data recovery operations simultaneously. Additionally, error-free data from the tested PE_i or the data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific PE_{i+1} for subsequent testing.

	0	1	2	3
0	128	128	64	255
1	128	64	255	64
2	64	255	64	128
3	255	64	128	128

Cur_pixel

	0	1	2	3
0	1	1	2	3
1	1	2	3	4
2	2	3	4	5
3	3	4	5	5

Ref_pixel

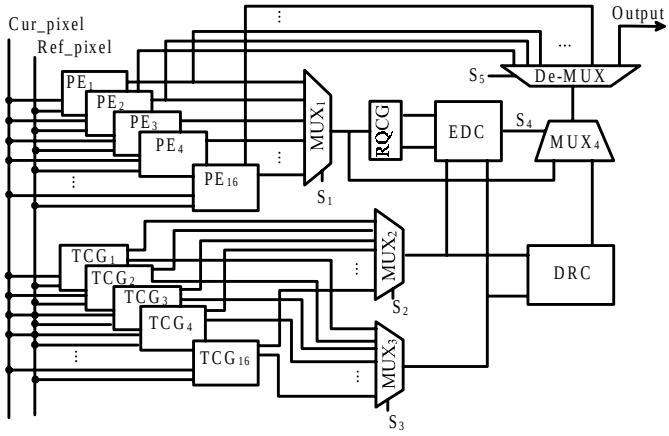
D. Numerical Example

A numerical example of the 16 pixels for a 4X 4 macroblock in a specific PE_i of a ME is described as follows. Fig. 5 presentsexample of pixel values of the Cur_pixel and Ref_pixel. Based on (7), the SAD value of the 4X4 macroblock is

$$SAD = \sum_{i=0}^{3}\sum_{j=0}^{3}\left|X_{ij} - Y_{ij}\right|$$
$$= \left|X_{00} - Y_{00}\right| + \left|X_{o1} - Y_{o1}\right| + ... + \left|X_{33} - Y_{33}\right|$$
$$= (128\ 1) + (128\ 1) + ...(128\ \ 5)$$
$$= 2124$$

According to the description of RQ code in Section II, the modulo is assumed here to be $m = 2^6 1 = 63$ Thus, based on (8) and (9), the RQ code of the SAD value shown in (14) are $R_T = R_{PE_i} = |2124|_{63} = 45$ and $Q_T = Q_{PE_i} = \lfloor 2124/63 \rfloor = 33$. Since the value of $R_T(Q_T)$ is equal to $R_{FEi}(Q_{FE_i})$ EDC is enabled and a signal "0" is generated to describe a situation in which the specific is PE_i .e. the pixel values of PE_i .

Fig. 6. Proposed EDDR architecture design for a ME. $2124 = 100001001100_2$ is turned into $77 = 000001001101_2$, resulting in a transformation of the RQ code of R_{PE_i} and Q_{PE_i} into $|77|_{63} = 14$ and $\lceil 77/63 \rceil = 1$. Thus, an error signal "1" is generated from EDC and sent to the MUX in order to select the recovery results from DRC.



E. Overall Test Strategy

By extending the testing processes of a specific PE_i in Fig. 2, Fig. 6 illustrates the overall EDDR architecture design of a ME. First, the input data of Cur_pixel and Ref_pixel are sent simul- taneously to PEs and TCGs in order to estimate the SAD values and generate the test RQ code R_T and Q_T Second, the SAD value from the tested object PE_i, which is selected by MUX_1, and Q_{PE_i} codes. Meanwhile, the corresponding test codes R_{T_i} and Q_{T_i}, from a specific TCG_i are selected simultaneously by MUXs 2 and 3, respectively. Third, the RQ code from TCG_i and RQCG circuits are compared in EDC to determine whether the tested object PE_i have errors. The tested object PE_i is error – free if and only if $R_{PE_i} = R_{T_i}$ and $Q_{PE_i} = Q_{r_i}$. Additionally, DRC is used to recover data encoded by TCG_i, i.e. the appropriate R_{T_i} and Q_{T_i} codes from TCG_i are selected by MUXs 2 and 3, respectively, to recover data. Fourth, the error-free data or data recovery results are selected by MUX_4 Notably, control signal S_4 is generated from EDC, indicating that the comparison result is error-free $(S_4 = 0)$ or errancy $(S_4 = 1)$. Finally, the error-free data or the data-recovery re- sult from the tested object FE_i is passed to a De-

MUX, which is used to test the next specific PE_{i+1}; otherwise, the final result is exported.

IV. RESULTS AND DISCUSSION

Extensive verification of the circuit design is performed using the VHDL and then synthesized by the Synopsys Design Com- piler with TSMC $0.18-\mu m$ 1 P6M CMOS technology to demon- strate the feasibility of the proposed EDDR architecture design for ME testing applications.

A. Experimental Results

Table I summarizes the synthesis results of area overhead and time penalty of the proposed EDDR architecture. The area is es- timated based on the number of gate counts. By considering 16 PEs in a ME and 16 TCGs of the proposed EDDR architecture, the area overhead of error detection, data recovery, and overall EDDR architecture $(AO_{FD}, AO_{DR}, \text{and } AO_{EDDR})$ are

$$AO_{ED} = \frac{1779 + 3265 \times 16 + 667}{69482 \times 16} = 4.92\% \quad .....(15)$$

$$AO_{DR} = \frac{3265 \times 16 + 2376}{69482 \times 16} = 4.91\% \quad .....(16)$$

$$AO_{EDDR} = \frac{1779 + 667 + 3265 \times 16 + 2376}{69482 \times 16} \quad ....(17)$$

$$= 5.13\%$$

The time penalty is another criterion to verify the feasibility of the proposed EDDR architecture. Table I also summarizes the operating time evaluation of a specific PE_i and each com- ponent in the proposed EDDR architecture. The following equa- tions show the time penalty of error detection and data recovery $(TP_{ED} \text{ and } TP_{DR})$ operations for a 4×4 macroblock (a PE_i with 16 pixels):

TABLE I

ESTIMATION OF AREA OVERHEAD AND TIME PENALTY

Components	PE	RQCG	EDC	TCG	DRC
Area (Gate counts)	69482	1779	667	3265	2376
Operation time (ns)	973.76	10.17	6.02	1016.56	17.99
Area Overhead(%)		5.13			
Time Penalty (%)		6.24			

$$TP_{ED} = \frac{(1016.56 + 6.02) 973.76}{937.76} = 5.01\% \quad .....(18)$$

$$TP_{DR} = \frac{(1016.56 + 17.99) - 973.76}{973.76} = 6.24\% \quad .....(19)$$

Notably, each PE of a ME is tested sequentially in the proposed EDDR architecture. Thus, if the proposed EDDR architecture is embedded into a ME for testing, in which the entire timing penalty is equivalent to that for testing a single PE., i.e. approx- imately about 5.01% and 6.24% time penalty of the operations of error detection and data recovery, respectively.

Notably, the operating time of the RQCG circuit can be ne- glected to evaluate TP_{ED} because TCG covers the operating time of RQCG. Additionally, the error-free/ errancy signal from EDC is generated after 1022.58 ns $(1016.56 + 6.02)$. Thus, the error-free data is selected directly from the tested object PE_i because the operating time of the tested object PE_i is faster than the results of data recovery from DRC.

B. Performance Discussion

The TCG component plays a major role in the pro- posed EDDR architecture to detect errors and recover data. Additionally, the number of TCGs significantly influences the circuit performance in terms of area overhead and throughput. Figs. 7 and 8 illustrate the relations between the number of TCGs, area overhead and throughput. The area overhead is less than 2% if only one TCG is used to execute; however, at this time, the throughput is extremely small. Notably, the throughput of a ME without embedding the proposed EDDR architecture is about 25 800 kMB/s. Fig. 8 clearly indicates that the throughput is around 25 000 kMB/s, if the proposed EDDR architecture with 16 TCGs is embedded into a ME for testing. Thus, to maintain the same throughput as much as possible, 16 TCGs must be adopted in the proposed EDDR architecture for a ME testing applications. Although the area overhead is increased if 16 TCGs used (see Fig. 7), the area overhead is only about 5.13%, i.e. an acceptable design for circuit testing.

This work also addresses reliability-related issues to demon- strate the feasibility of the proposed EDDR architecture. Relia- bility is the probability that a component or a system performs its required function under different operating conditions en- countered for a certain time period [24]. The constant failure- rate reliability model

$$R(t) = e^{-\lambda t} = e^{-\lambda_b \Pi_T \Pi_q \Pi_k t} = e^{-\left(\frac{1500}{T^{1.5}}\right) G^{\frac{5}{T^{1.5}}} \Pi_T \Pi_q \Pi_k t} \quad ..(20)$$

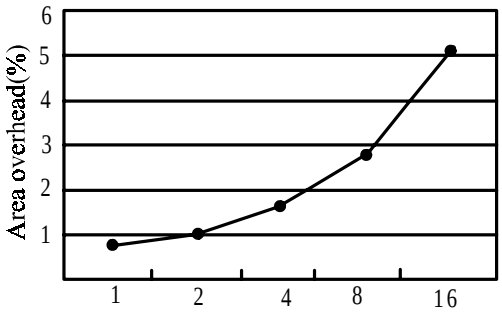


Fig. 7. *Relation between TCG and area overhead.*

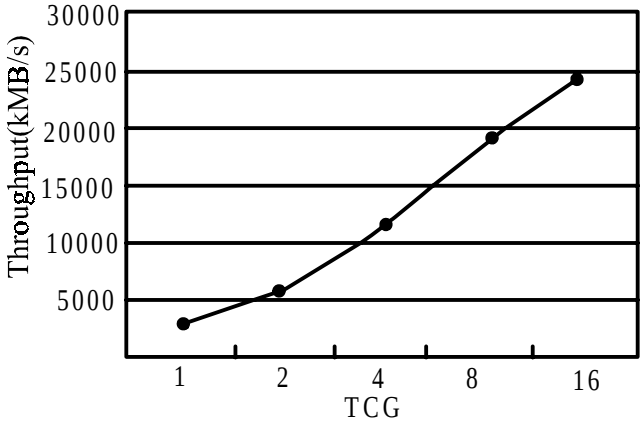


Fig. 8 : *Relation between TCG and throughput.*

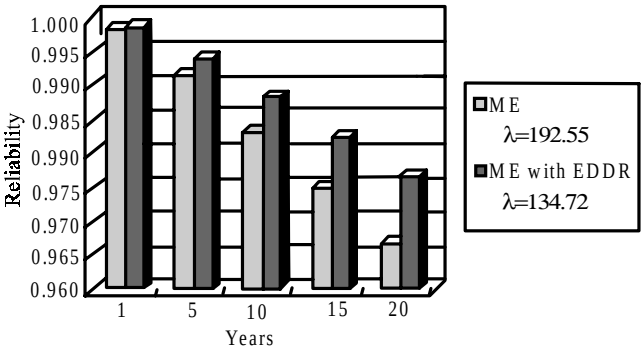


Fig. 9 : *Failure-rate and reliability analysis.*

is used to estimate the reliability of the proposed EDDR archi- tecture for ME testing applications, where λ denotes the failurerate; λ_b represents the base failure – rate of MOS digital logic, G refers to Gate count; $\prod_T = 1.0(25^oC)$; $\prod_Q = 1.0$ (hermetic package); and $\prod_T = 1.0$ (ground benign environment).

The failure – rate λ in (20) can be expressed as the ratio of the total number of failures to the total operating time, i.e. failure- rate in time (FIT), which represents the number of failures per 10^9 device hours of accelerated stress tests [25]. Notably, the total operating time, T in λ_b can be expressed as the year of manufacturing. Since the proposed EDDR architecture is syn- thesized by using TSMC 0.18mμ 1P6M CMOS technology, 1998 is given as the year of manufacturing for a wide variety of components. Thus, T is defined as 12 years, because the year of manufacturing is 1998. Fig. 9 clearly indicates that the low failure-rate and high reliability levels can be obtained if the pro- posed EDDR architecture is embedded into a ME for testing applications.

V. CONCLUSION

This work presents an EDDR architecture for detecting the errors and recovering the data of PEs in a ME. Based on the RQ code, a RQCG-based TCG design is developed to generate the corresponding test codes to detect errors and recover data. The proposed EDDR architecture is also implemented by using VERILOG and synthesized by the Synopsys Design Compiler with TSMC 0.18- m 1P6M CMOS technology. Experimental results indicate that that the proposed EDDR architecture can effectively detect errors and recover data in PEs of a ME with reasonable area overhead and only a slight time penalty. Throughput and reliability issues are also discussed to demonstrate the satisfactory performance of the proposed EDDR architecture design for ME testing applications.

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Novel Bandpass Filter Using Coupled Line for WLAN Applications

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ABSTRACT

A novel planar band-pass filter design using edge coupled micro-strip line filt is presented for Wireless local area network (WLAN) applications. The filter, comprising three micro-strip coupled lines and taper, capable of generating a resonant mode with good impedance matching conditions. The simulated and measured results have a midband at 5GHz and bandwidth of 0.150GHz. Passband insertion and return loss is specified to be <5dB and >10dB respectively, covering the WLAN bands and insertion loss was large, which was 3.67 dB at centre frequency of filter.

Index Terms

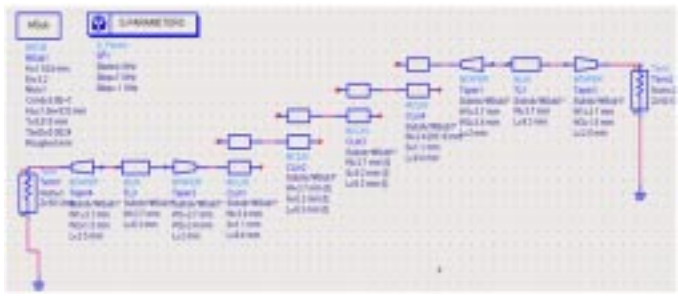
Bandpass filter, edge coupled line resonator, WLAN.

I. INTRODUCTON

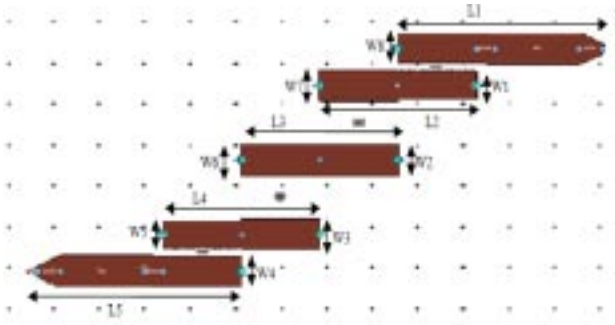
Microwave filters have aroused widespread applications, especially in low power wireless communication gadgets. In the era of modern wireless communication systems, multiband filters play a vital role [1]. The currently popular design is suitable for wireless local area network (WLAN) operation in the 2.4 GHz (2.4–2.484 GHz) and 5.2/5.8 GHz (5.15–5.35 GHz/5.725–5.825 GHz). To meet the demand in modern wireless communications, microwave filters have become attractive components with low cost and compact size. Many approaches have been reported in the literature to design bandpass filters (BPFs). In general, resonators or stubs were adopted widely to produce several transmission zeros for filter design, such as the open stub [3], open-loop ring resonators [2], and stepped-impedance stubs [4], and the stepped-impedance resonator (SIR) [5]. In this paper, a new single layered substrate filter design is proposed using coupled strip line resonators for the achievement of WLAN mode operation as illustrated in Figure 1(a). The filter is capable of generating a passband with good impedance matching conditions and huge insertion loss at centre frequency 5 GHz. The design of proposed filter and its performance both from simulation and practical are presented in the following sections.

II. PROPOSED FILTER DESIGN

Figure 1 shows the geometry of the proposed finite ground bandpass filter, designed using Advance Design System (ADS). And simulated using s-parameter for momentum and EMDS simulation. Finally, the designed layout of coupled line filter was fabricated on NH9320 substrate having dielectric constant $\in r = 3.2$ and 1.524 mm thickness (15 to 18 μm copper thickness, dissipation factor of 0.0024) using dry etching technique. Four tapers used to provide the proper impedance matching mentioned with width and length in the figure1 (a). And the space between the couplings is also shown in figure 1(a). The other geometric parameters of the filter are as L1 = 23.2 mm, L2 = 18.7 mm, L3 = 18.6 mm, L4 = 18.7 mm, L5 = 23.2 mm and the width w1 = w8 = 3.42 mm, w2 = w7 = 3.7 mm, w3 = w6 = 3.7 mm, w4 = w5 = 3.4 mm mentioned in Figure 1(b).



(a)



(b)

Figure1 Geometry of the bandpass filter. (a) Schematic of coupled line band pass filter at 5GHz.(b) Layout of the bandpass filter.

As in the layout, there is relatively large spacing, so the coupling is very weak and therefore, insertion loss was large. To investigate the performance of the proposed filter configurations in terms of achieving bandpass operation, an Advanced Design System (ADS) for high frequency structure simulation is used and the same filter is fabricated and results were measured to verify the simulations, was used for the required numerical analysis using line calculators to obtain the proper geometrical parameters from even and odd impedances and characteristic impedances keeping electrical length 90 degree. [6]

III. RESULTS AND DISCUSSION

Simulation is done using both EMDS and momentum method. Simulated result at 5GHz using EMDS is shown in figure 2. The return loss obtained is 16.408 dB and insertion loss –11.756 dB at 5GHz. This is optimized to get better result after simulation in layout window.

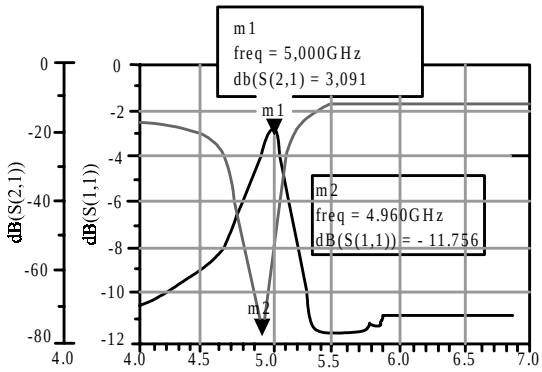
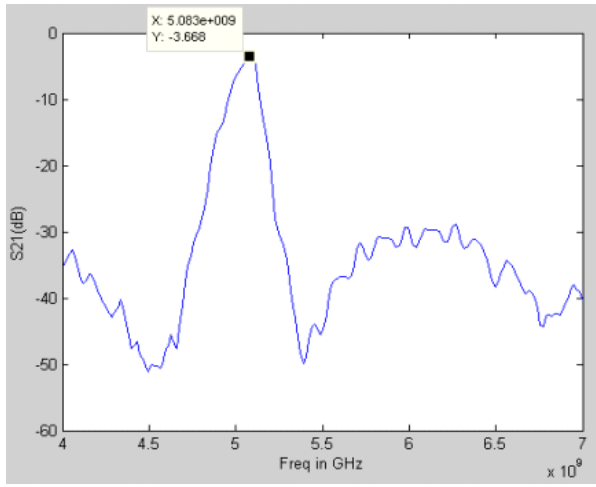


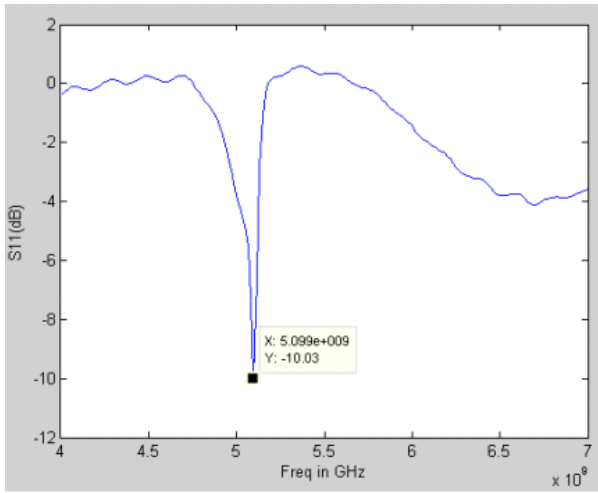
Figure 2 : *Simulated Return Loss of the proposed filter using EMDS.*

Fabricated filter on NH9320 substrate then tested on Vector Network Analyser (VNA) as illustrated in figure 3. With start frequency 0.5 GHz and stop frequency to 7 GHz. Then VNA was calibrated for TMSO for two channels. And the measured results are shown in figure 4.

Figure 3 : *Setup for measurement of S paprameters of proposed filter.*



(a)



(b)

Figure 4 : *Measured results of filter using VNA (a) S21 parameter (b) S11 Parameter*

As figure 3 depict that there is a shift of 0.083GHz in frequency from designed and simulated centre

frequency 5GHz. measured bandwidth and quality factor are approximately 0.119GHz and 43.

IV. CONCLUSION

A bandpass filter for WLAN bands is proposed. The various parameters of the filter are optimized through simulation. Simulated and measured bandpass coupled line filter presented here is specified to have a mid-band at 5GHz and bandwidth of 0.150GHz i.e 3%. Passband insertion and return loss is specified to be <5dB and >10dB respectively. There is relatively large spacing, so the coupling is very weak and therefore, insertion loss was large. The proposed filter is a narrow band filter, so it can be used as resonator in the feedback path of feedback oscillator for frequency stabilization.

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Double Error Correcting Data Negative Codes

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ABSTRACT

Error Correcting Codes play an important role in maintaining a reliable link the communication system. Error correcting codes are used to protect the syste... against errors introduced due to various reasons in the transmission media. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data. To achieve the acceptable error rate Forward error correction (FEC) control is done where received error rate is Controlled via Forward Transmission only. An (n,k) Linear Block Code with a specified Parity bit format expresses a Block of 'k' message bits into a Block of 'n' Coded bits. In Systematic Linear Block code 'k' information bits are followed by 'n-k=r' parity bits forming an 'n' bit Code word. In this paper, a new Systematic Double Error Correcting Linear Block Code is proposed called the Data Negation codes.

Index Terms

Systematic Block Codes, Code Rate, Weight Enumerator, Binary Symmetric Channel , Probability of Undetected Errors.

I. INTRODUCTION

Channel coding refers to the class of signal transformations designed to improve the communications performance. It enables the transmitted signals to better withstand the effects of channel noise. The redundancy inserted into the source data makes the detection of errors present and the correction of errors feasible. These Codes enable the communication systems to have a reliable transmission over noisy channels. Error correcting codes are algorithms for expressing a sequence of numbers such that any errors which are introduced can be detected and corrected based on the remaining numbers. These codes are Forward Error Correction codes where the error rate is controlled via forward transmission only. The (n,k) Block Code consists of q^k number of Code words. As q = 2 ,the Code words contain Binary numbers '0' and '1'. In Systematic Linear Block code 'k' information bits are followed by 'n-k = r' parity bits forming an 'n' bit Code word. The parity bits are generated in accordance with a specified Encoding rule which gives the structure of these parity bits. For a general case of Linear Block Codes ,all the 'n' Code words are formed by linear combinations of 'k' message bits. Systematic Code is a special case where the first k digits of the Code are the data bits and the last n-k bits are the Parity check bits formed by linear combination of data bits[1]. Hence in a Systematic Code the message bits are transmitted without alteration. The weight of (n,k) code is the number of nonzero elements present in it [2]. The Code rate of (n,k) code is defined as "(k/n)x100" and is less than 100%. At the decoding stage ,for a given Transition probability, some erroneous digits pass through the decoder undetected. This probability is indicated by Probability of Undetected Error In this paper a new Systematic Double Error Correcting Linear Block Code is proposed called the Data Negation codes. The Probability of Undetected Error is calculated using MacWilliams Identities.

II. GENERATION OF CODEWORD

These codes are weight based codes represented as (n+1,k) codes with coding efficiency of less than 50%. The encoding procedure depends on weight of the message. The weight of the message is the number of 1's present. In Systematic Block Codes the parity bits are the linear combination of message bits. In Data Negation codes the parity bit structure is not the same for all the codes because the weight is not same for all messages. These codes are also referred as Systematic Codes with unequal Parity Bit Structure.

The general form of the (n+1,k) Data Negation Code word is given by $M_1M_2.....M_kP_1P_2.....P_kP_{k+1}$ where $M_1M_2.....M_k$ are the k message bits and $P_1P_2.....P_k$ are (n-k) parity bits where n = 2k+1 and P_{k+1} is the Modulo-2 addition of the message bits [3].

The Polynomial description of the Code word is given as C(x) = M(x).P+Q(x), where M(x) is the message polynomial and P is the Primary matrix of order [kx2K] and Q(x) is the secondary polynomial. The Primary Matrix is same for the message with Zero/Even weight and odd weight. It is given as the first row of 'P' is $1+x^{k+1}$, second row is $x+x^{k+1}$, third row is x^k+x^{k+3} and the k^{th} row is x^k+2^{2k}.

The Secondary Polynomial is Q(x) and for message with Zero/Even weight is given by Q(x) = 0 which is written as $0.x^0+0.x^1+....0.x^k+0.x^{k+1}+0.x^{k+2}+0.x^{k+3}+.....+0.x^{2k}$ The Secondary Polynomial for message with Odd weight is given by

$$Q(x)=0.x^0+0.x^1+...0.x^k+1.x^{k+1}+1.x^{k+2}+1.x^{k+3}+....+1.x^{2k}.$$

For an (n,k) Code the message polynomial is $M(x)=M_1.x^0+M_2.x^1+....M_k.x^k$ .The Code polynomial is given as

$$C(x)=M_1.x^0+M_2x^1+...M_k.x^k+P_1.x^{k+1}+P_2.x^{k+2}+....P_k.x2^k$$

In the Matrix form, the code word of 'n' bits length is given by C = M.P+Q, where 'M' is the message word, 'P' is the Primary Matrix of order (kx2k) and 'Q' is the Secondary Matrix of order (1x2k).

For the message words of zero/even weight, $P=[I_{kxk},I_{kxk}]_{kx2k}$ and $Q=[\{00.....\}_{1xk}\{00....\}_{1xk}]_{1x2k}$ For the message word of odd weight, Primary Matrix being the same and $Q=[\{00.....\}_{1xk}\{11....\}_{1xk}]_{1x2k}$ The code word is obtained as $[M_1M_2.....M_kP_1P_2....P_kP_{k+1}]$. The Parity bits are obtained from the relation

- For the message word of zero/even weight, $P_1=M_1+0;P_2=M_2+0;..P_k=M_k+0$.
- For the message word with odd weight, $P_1=M_1+1,P_2=M_2+1;..P_k=M_k+1$. Thus, the encoding rule is
- for the message words with Zero/even weight, the parity bits of the corresponding code word are same as the message bits.
- For the message words with Odd weight, the parity bits of the corresponding code word is the complement of the message bits. Hence the name is Data Negation codes.

All the code words with even Message word length will satisfy the relation $C.P^T=P.C^T=[000..0]_{1xk}$ .All the code words with odd Message word length will satisfy the relation $C.P^T=P.C^T=[111..1]_{1xk}$,where C^T and P^T are the transposed versions of the primary Matrix and the code vector C. If the length of the message bits is 5 then 5 parity bits are added according to the weight of the message word.

III. DOUBLE ERROR DETECTION CAPABALITY

These weight based codes can be used for the detection of single errors and Double errors. Let the received code word be

$$R[M_1M_2...M_k\ P_1P_2..P_kP_{k+1}]$$

The Parity bits of the received code word are Modulo-2 added with the Message bits, i.e.

$$\begin{array}{l} M_1\ M_2\ M_3.....M_K \\ +\ \ +\ \ +\ .....+ \\ P_1\ \ P_2\ \ P_3.....P_K \\ \hline \text{Modulo}-2\text{ added Sum (Length is of k bits)} \end{array}$$

The structure of the Parity bits is decided based on the Modulo-2 added sum.

If the parity bits of the received code word are same as message bits,

(i) Under error free reception, the above Modulo-2 added sum consists of all zeros.

(ii) Under the reception with single error, the above Modulo-2 added sum consists of (k-1) number of 0's

and a single 1.

If the Parity bits of the received code word are the Complements of the message bits,

(i) Under error free reception, the above Modulo-2 added sum consists of all ones.

(ii) Under the reception with single error, the above Modulo-2 added sum consists of (k-1) number of 1's and a single 0.

If this sum consists of a single 1 and (k-1) number of zeros or a single 0 and (k-1) number of 1's, it indicates the presence of single error in the received code word. The occurrence of the single error can be detected using the Data Negation Codes.

If this sum consists of 2 number of 1's and (k-2) number of zeros or 2 number of 0's and (k-2) number of 1's, it indicates the presence of double error in the received code word. The double errors occurring in some random bit pairs in the received code can be corrected by making the code as (n+1,k) code .One extra parity bit is added which is the Modulo-2 added sum of 'k' message bits. The proposed code can correct single bit error and (M_i, P_j) random double bit pairs in the received code word where i = 1,2,….k and j = 1,2,…..k. Also the condition for the index is i<j,k+1 and i<j.

IV. ERROR DETECTION AND CORRECTION

Under error free reception the received code word will satisfy (k+2) number of conditions. These conditions are the Modulo-2 sum of the message and parity bits along with the extra parity bit added. Considering the bit positions in the received code word (1 indicating M_1, 2 indicating M_2,….etc)

The condition for odd length message word

- For the code word whose message word is of zero/ even weight

1) 1+(k+1) = 0

2) 2+(k+2) = 0

3) ……

K+1) 1+2+3+…+k+(2k+1) = 0

K+2) (k+1)+(k+2)+……(2k+1) = 1

- For the code word whose message word is of odd weight

1) 1+(k+1)=1

2) 2+(k+2)=1

3) ……

K+1) 1+2+3+…+k+(2k+1) = 0

K+2) (k+1)+(k+2)+……(2k+1) = 0

The condition for even length message word

- For the code word whose message word is of zero/ even weight

1) 1+(k+1) = 0

2) 2+(k+2) = 0

3) ……

K+1) 1+2+3+…+k+(2k+1) = 0

K+2) (k+1)+(k+2)+……(2k+1) = 0

- For the code word whose message word is of odd weight

1) 1+(k+1) = 1

2) 2+(k+2) = 1

3) ……

K+1) 1+2+3+…+k+(2k+1) = 0

K+2) (k+1)+(k+2)+……(2k+1) = 0

Any deviation from the above conditions indicates the presence of error in the received code word. For the received code the above conditions are computed .For the occurrence of Double error

* The position number commonly present in (k+1)th condition and the jth condition in error (j being the lowest of the two present where j=1,2,…k) will give the position of the message bit that is in error.

* The position number commonly present in (k+2)th condition and the jth condition in error (j being the highest of the two present where j=1,2,…k) will give the position of the parity bit that is in error.

For the occurrence of single error

* The position number commonly present in (k+1)th condition and the jth condition in error will give the position of the message bit in error.

* The position number commonly present in (k+2)th condition and the jth condition in error will give the position of the parity bit in error.

The deviation from error free condition indicates the presence of errors. The conditions differing are " ERROR CONDITIONS" represented by "E" and the "CORRECT CONDITIONS" are represented by "C".

V. ILLUSTRATIONS

1. Let the received code word of (11,5) code b

$$R = M_1, M_2, M_3, M_4, M_5, P_1, P_2, P_3, P_4, P_5, P_6 = 00111010110$$

The structure of parity is checked using the Modulo-2 addition of the message bits and the parity bits.

$$\begin{array}{c} 0\ 0\ 1\ 1\ 1 \\ +\ +\ +\ +\ + \\ 0\ 1\ 0\ 1\ 1 \\ \hline 0\ 1\ 1\ 0\ 0 \end{array}$$

Modulo-2 sum consists of two number of 1's and (k-2) zeros and indicates that the parity bits are same as message bits and weight of the message word is even. Two number of ones indicates double error.

Applying the Error free conditions for R

- M1+P1 = 0—C—(1)
- M2+P2 = 1—E—(2)
- M3+P3 = 1—E—(3)
- M4+P4 = 0—C—(4)
- M5+P5 = 0—C—(5)
- M1+M2+M3+M4+M5+P6 = 1—E—(6)
- P1+P2+P3+P4+P5+P6 = 1——E——(7)

The bit commonly present in 6^{th} condition and the 2^{nd} condition (2 being the lowest of the two present where j = 2,3) is M2 and indicates that it is in error.

The bit commonly present in 7^{th} condition and the 3^{rd} condition (3 being the highest of the two present where j = 2,3) is P3 and indicates that it is error.

Hence the bit pair (M2,P3) is in error and the corrected R = 01111011110

2. Let the received code word of (11,5) code be

$$R = M_1, M_2, M_3, M_4, M_5, P_1, P_2, P_3, P_4, P_5, P_6 = 10111110011$$

The structure of parity is checked using the Modulo-2 addition of the message bits and the parity bits.

$$\begin{array}{c} 1\ 0\ 1\ 1\ 1 \\ +\ +\ +\ +\ + \\ 1\ 1\ 0\ 0\ 1 \\ \hline 0\ 1\ 1\ 1\ 0 \end{array}$$

Modulo-2 sum consists of two number of 0's and (k-2) ones and indicates that the parity bits are complement of the message bits and weight of the message word is odd.

Applying the Error free conditions for R

- M1+P1 = 0—E—(1)
- M2+P2 = 1—C—(2)
- M3+P3 = 1—C—(3)
- M4+P4 = 1—C—(4)
- M5+P5 = 0—E—(5)
- M1+M2+M3+M4+M5+P6 = 1—E—(6)
- P1+P2+P3+P4+P5+P6 = 0——E——(7)

The bit commonly present in 6^{th} condition and the 1^{st} condition (1 being the lowest of the two present where j = 1,5) is M1 and indicates that it is in error.

The bit commonly present in 7^{th} condition and the 5^{th} condition (5 being the highest of the two present where j = 1,5) is P5 and indicates that it is error.

Hence the bit pair (M1,P5) is in error and the corrected R= 00111110001.

3. Let the received code word of (11,5) code be

$$R = M_1, M_2, M_3, M_4, M_5, P_1, P_2, P_3, P_4, P_5, P_6 = 00011111101$$

The structure of parity is checked using the Modulo-2 addition of the message bits and the parity bits.

$$\begin{array}{c} 0\ 0\ 0\ 1\ 1 \\ +\ +\ +\ +\ + \\ 1\ 1\ 1\ 1\ 0 \\ \hline 1\ 1\ 1\ 0\ 1 \end{array}$$

Modulo-2 sum consists of single number of 0 and (k-1) ones and indicates that the parity bits are complement of message bits and weight of the message word is odd. Single 0 indicates the occurrence of single bit error.

Applying the Error free conditions for R

- M1+P1 = 1—C—(1)
- M2+P2 = 1—C—(2)
- M3+P3 = 1—C—(3)
- M4+P4 = 0—E—(4)
- M5+P5 = 1—C—(5)
- M1+M2+M3+M4+M5+P6 = 1—E—(6)
- P1+P2+P3+P4+P5+P6 = 1——C——(7)

The bit commonly present in 6^{th} condition and the 4^{th} condition is M4 and indicates that it is in error. Hence the single bit M4 is in error and the corrected

R = 00001111101

VI. WEIGHT ENUMERATOR AND PROBABILITY OF UNDETECTED ERROR

Undetected errors occur when the Decoder fails to detect the presence of errors. If the coding scheme is used for error detection on a Binary Symmetric Channel, the Probability of an undetected Error $P_{ud}(E)$ is obtained from the weight enumerator of the code {Ai}. If the code 'C' contains Ai number of code words of weight 'i' the weight Enumerator A(z) of the code is defined as

$$A(z) = \sum_{i=0}^{n} Ai.z^{i}$$

Using Mac Williams identity, the probability of undetected error is computed from A(z) and is given as

$$P_{ud}(E) = (1-p)^{n}.\sum_{i=1}^{n}[A[p/(1-p)]-1] \text{ where } z = p/1-p$$

Where p is the Transition probability. It is the probability that a transmitted '0' is received as '1' and vice-versa.

N is the number of code bits in the Code word. The set of weight distributions for an (11,5) DN code is $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}\} = \{1, 0, 0, 0, 10, 0, 15, 0, 5, 0, 0, 0\}$ i.e. the No. of Code words of zero weight =1,No.of code words of weight four = 10, No. of code words of weight five = 1, No. of code words of weight Six = 15, No. of code words of weight Eight = 5.

The weight Enumerator of the code is

$$A(z) = 1 + 10z^{4} + z^{5} + 15z^{6} + 5z^{8}$$

The Probability of the undetected error is

$$P_{ud}(E) = (1-p)^{11}\left[1 + 10(p/1-p)^{4} + (p/1-p)^{5} + 15(p/1-p)^{6} + 5(p/1-p)^{8} - 1\right]$$

The $P_{ud}(E)$ calculations for different Transition Probabilities(p) are as follows:

p	10^{-1}	10^{-2}	10^{-3}	10^{-4}
$P_{ud}(E)$	4.925×10^{-1}	9.331×10^{-5}	9.931×10^{-9}	1.109×10^{-12}

It is seen that for a transition probability of 10^{-4} over a BSC, the $P_{ud}(E)$ tells that ,out of 10^{12} code digits, there are on average 2 erroneous digits that pass through the decoder undetected when (11,5) Data Negation code is used.

VI. CONCLUSION

In this paper, a new Systematic Double Error Correcting Linear Block Code is proposed called the Data Negation codes. Random errors occurring up to Double errors can be detected.

In implementing the DN codes, complex mathematical rules are not required. Only Negation operation is used in generating the parity bits required for detection. Performance of DN code is checked in terms of $P_{ud}(E)$ Transmission of the data is done and Error rate is controlled using FEC. At the receiving end errors can be detected and corrected if proper decoding scheme is designed with minimum operations. The Coding efficiency of the proposed coding scheme is 47%.The code rate increases as the number of data bits are increased. The increasing demand of improved data rate and reliability in modern wireless communication systems is pushing next-generation standards toward error correction techniques with good performance.

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An Embedded Real - Time Finger - Vein Recognition System for Mobile Devices

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ABSTRACT

In consideration of emerging requirements for information protection ,biometric which uses human physiological or behavioral features for personal identification, has been extensively studied as a solution to security issues. However, most existing biometric systems have high complexity in time or space or both, and are thus not suitable for mobile devices. In this paper, we propose a real-time embedded finger-vein recognition system for authentication on mobile devices.

The system is implemented on a DSP platform and equipped with a novel finger-vein recognition algorithm. The proposed system takes only about 0.8 seconds to verify one input finger- vein sample and achieves an equal error rate (EER) of 0.07% on a database of 100 subjects. The experimental results demonstrate that the proposed finger-vein recognition system is qualified for authentication on mobile devices. [1]

I. INTRODUCTION

Private information is traditionally provided by using passwords or Personal Identification Numbers (PINs), which are easy to implement but is vulnerable to the risk of exposure and being forgotten. Biometrics, which uses human physiological or behavioral features for personal identification, has attracted more and more attention and is becoming one of the most popular and promising alternatives to the traditional password or PIN based authentication techniques [1]. Moreover, some multimedia content in consumer electronic appliances can be secured by biometrics [2]. There is a long list of available biometric patterns, and many such systems have been developed and implemented, including those for the face, iris, fingerprint, palmprint, hand shape, voice, signature, and gait. Notwi-thstanding this great and increasing variety of biometrics patterns, no biometric has yet been developed that is perfectly reliable or secure.

The great challenge to biometrics is thus to improve recognition performance in terms of both accuracy and efficiency and be maximally resistant to deceptive practices.

To this end, many researchers have sought to improve reliability and frustrate spoofers by developing biometrics that are highly individuating; yet at the same time, present a highly complex, hopefully insuperable challenge to those who wish to defeat them [4]. Especially for consumer electronics applications, biometrics authentication systems need to be cost-efficient and easy to implement [5].

The finger-vein is a promising biometric pattern for personal identification in terms of its security and convenience [6]. Compared with other biometric traits, the finger-vein has the following advantages [7]: (1) The vein is hidden inside the body and is mostly invisible to human eyes, so it is difficult to forge or steal. (2) The non-invasive and contactless capture of finger-veins ensures both convenience and hygiene for the user, and is thus more acceptable. (3) The finger-vein pattern can only be taken from a live body. Therefore, it is a natural and convincing proof that the subject whose finger-vein is successfully captured is alive.

We designed a special device for acquiring high quality finger-vein images and propose a DSP based embedded platform to implement the finger-vein recognition system in the present study to achieve better recognition performance and reduce computational cost.

II. OVERVIEW OF THE SYSTEM

The proposed system consists of three hardware modules: image acquisition module, DSP mainboard, and human- machine communication module. The structure diagram of the system is shown in Fig. 1. The image acquisition module is used to collect finger-vein images The DSP mainboard including the DSP chip, memory

(flash), and communication port is used to execute the finger-vein recognition algorithm.communicate with the peripheral device. The human- machine communication module (LED or keyboard) is used to display recognition results and receive inputs from users.

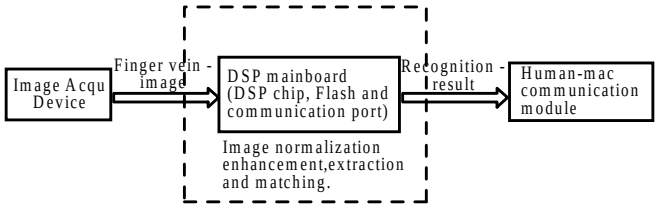

Fig.1 : *The hardware diagram of the proposed system.*

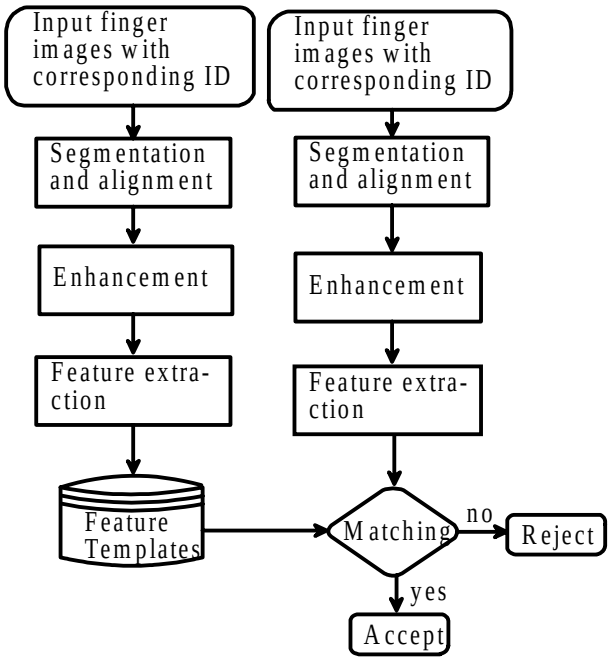

Fig.2 : *The flow-chart of the proposed recognition algorithm.*

The proposed finger-vein recognition algorithm contains two stages: the enrollment stage and the verification stage. Both stages start with finger-vein image pre-processing, which includes detection of thregionofinte rest (ROI), image segmentation, alignment, and enhancement For the enrollment stage, after the pre-processing and the feature extraction step, the finger-vein template database is built. For the verification stage, the input finger-vein image is matched with the corresponding template after its features are extracted. Fig. 2 shows the flow chart of the proposed algorithm. Some different methods may have been proposed for finger-vein matching.

III. IMAGE ACQUISITION

To obtain high quality near-infrared (NIR) images, a special device was developed for acquiring the images of the finger-vein without being affected by ambient temperature. Generally, finger-vein patterns can be imaged based on the principles of light reflection or light transmission [8]. We developed a finger-vein imaging device based on light transmission for more distinct imaging.

Our device mainly includes the following modules: a monochromatic camera of resolution 580 × 600 pixels, daylight cut-off filters (lights with the wavelength less than 800 nm are cut off), transparent acryl (thickness is 10 mm), and the NIR light source. The structure of this device is illustrated in Fig. 3. The transparent acryl serves as the platform for locating the finger and removing uneven illumination.The NIR light irradiates the backside of the finger. In [9], a light-emitting diode (LED) was used as the illumination source for NIRlight.Withthe LED illumination source, however, the shadow of the finger-vein obviously appears in the captured images. To address this problem, an NIR laser diode (LD) was used in our system

Compared with LED, LD has stronger permeability and higher power. In our device, the wavelength of LD is 808 nm. Fig. 4 shows an example raw finger-vein image captured by using our device.

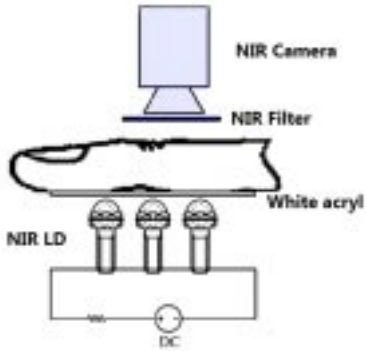

Fig. 3 : *Illustration of the imaging device.*

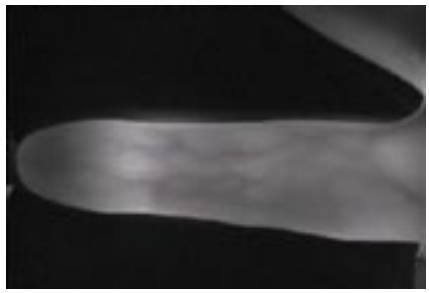

Fig. 4 : *An example raw finger-vein image captured by our device.*

IV. PROPOSED ALGORITHM

A. Image Segmentation and Alignment

Because the position of fingers usually varies across different finger-vein images, it is necessary to normalize the images before feature extraction and matching.

The bone in the finger joint is articular cartilage. Unlike other bones, it can be easily penetrated by NIR light. When a finger is irradiated by the uniform NIR light, the image of the joint is brighter than that of other parts.

Therefore, in the horizontal projection of a finger-vein image, the peaks of the projection curve correspond to the approximate position of the joints (see Fig.5).

Since the second joint of the finger is thicker than the first joint, the peak value at the second joint is less prominent. Hence, the position of the first joint is used for determining the position of the finger.

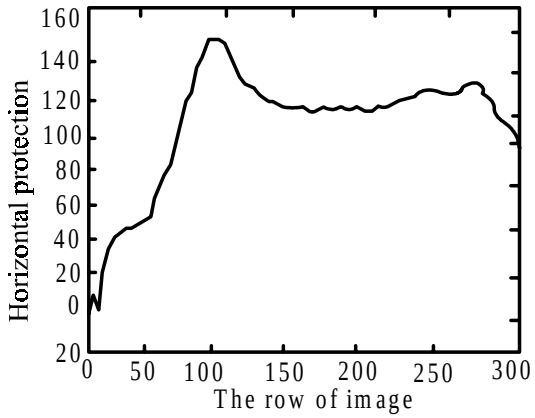

Fig. 5 : *Horizontal projection of the raw image.*

Fig.6 : *The segmented ROI of the finger-vein image.*

The alignment module includes following steps. First, the part between the two joints in the finger-vein image segmented based on the peak values of the horizontal projection of the image. Second, a Canny operator with locally adaptive threshold is used to get the single pixel edge of the finger. Third, the midpoints of finger edge are determined by edge tracing so that the midline can be obtained. Fourth, the image is rotated to adjust the midline of the finger horizontally.

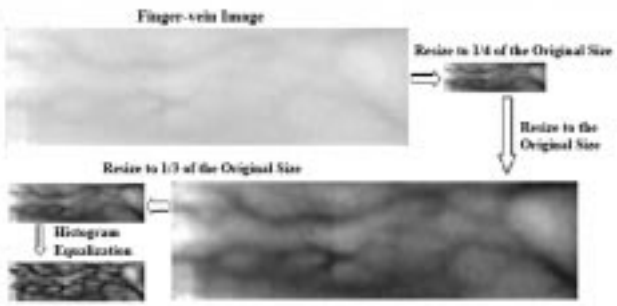

Fig. 7 : *The procedure of our method for image enhancement.*

B. Image Enhancement

The segmented finger-vein image is then enhanced to improve its contrast as shown in Fig. 7. The image is resized to 1/4 of the original size, and enlarged back to its original size. Next, the image is resized to 1/3 of the original size for recognition. Bicubic interpolation is used in this resizing procedure. Finally, histogram equalization is used for enhancing the gray level contrast of the image.

V. EXPERIMENTAL RESULTS

A. Dataset

To the best of our knowledge,is no public finger vein image database has yet been introduced. We constructed a finger-vein image database for evaluation, which contains finger-vein images from 100 subjects (55% male and 45% female) from a variety of ethnic/racial ancestries. The ages of the subjects were between 21 years old and 58 years old. We collected finger-vein images from the forefinger, middle finger, and ring finger of both hands of each subject. Ten images were captured for each finger at different times (summer and winter). Therefore, there were a total of 6,000 finger-vein images in the database. Fig.8 shows some example finger-veinfromdifferentfingers.

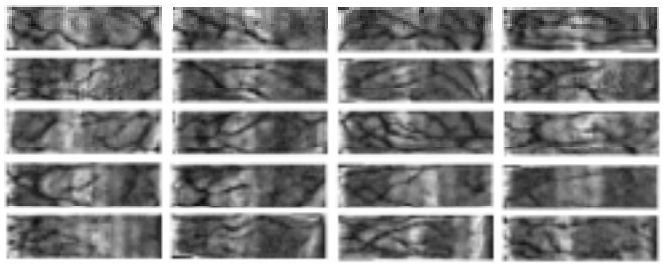

Fig. 8 : *Finger-vein images from different fingers after preprocessing*

B. Performance Evaluation

There are two types of errors in matching results in biometric verification. The first is false rejection, which claims a genuine pair as impostor, and the second is falseacceptance, which claims an impostor pair as genuine. These two types of errors are in a trade-off relationship. In biometrics, the performance of a system is evaluated by the EER (equal error rate). The EER is the error rate when the FRR (false rejection rate) equals the FAR (false acceptance rate) and is, therefore, suitable for measuring the overall performance of biometric systems because the FRR and FAR are treated equally.

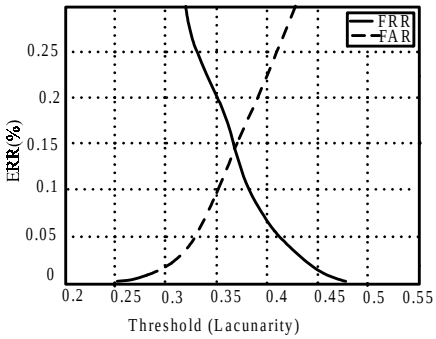

Fig. 9 : *The FAR and FRR curves of the methods based on (a) blanket dimension and (b) lacunarity, respectively*

The curves of FRR and FAR were used to evaluate theperformance of our proposed method. Fig. 9 shows the FAR and FRR curves corresponding to the two methods based on blanket dimension and lacunarity, respectively. From Fig. 9, it can be seen that the EER of the two methods are 0.155% and 0.146%, which are similar.

However, when the two kinds of features are combined, the ERR is decreased to 0.07%, as shown in Fig. 10.Because the proposed finger-vein recognition system is targeted for application in mobile devices, according to [18] the energy efficiency of the system is very important.

When the proposed system is idle, the power consumption of DSP is about 42.72milliwatts (mW), and the power consumption of the whole system is under 70 mW in standby mode. In full active model, the power consumption of the aforementioned model is 1636.4 mW. On average, the actual power consumption of the proposed system is no more than 1.5 watts.

The lower power consumption of the proposed system means that it is very efficient and is thus very suitablefor mobile consumer electronic devices.

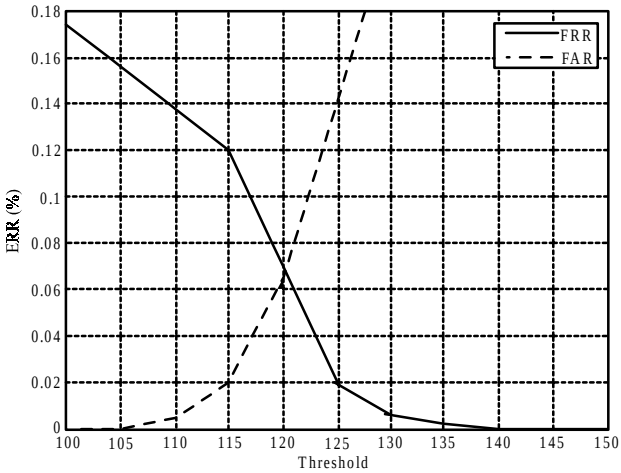

Fig.10 : *The FAR and FRR curves of the method combining the blanket dimension and lacunarity.*

C. Comparison with previous Methods

Miura et al. [19] used a database that contained 678 different infrared images of fingers. These images were obtained from persons working in their laboratory aged 20 to 40, approximately70% of whom were male. Song's [20] finger-vein image dataset contained 1,125 images collected using an infrared imaging device they built. Nine images were taken for each of 125 fingers. Compared with these databases, ours is larger and the data-collection interval is longer. Thus, our database is more challenging. Moreover, our system is implemented on a general DSP chip. Table 1 shows that the average times required for feature extraction and matching in our system are 343 ms and 13 ms, respectively. For the whole system, plus the time for is a little bit more complicated than that in Song's method, our system achieves an EER of 0.07%, indicating that our method significantly outperforms previous methods image capturing, the time required for the authentication of a user is less than 0.8 s. Although the feature extraction in our system is a little bit more complicated than that in Song's method,our system achieves an EER of 0.07% indicating that our method significantly outperforms previous methods.

Table 1

RECOGNITION RATE AND RESPONSE TIME

Method	Sample number#finger(#image per finger	EER(%)	time	
			Feature extractio	Matching
Our method	600(*10)	0.07	343ms	13ms
Miura s method	678(*2)	0.145	450ms	10ms
Song s	125(*9)	0.25	118ms	88ms

VI. CONCLUSION

The present study proposed an end-to-end finger-vein recognition system based on the blanket dimension and lacunarity implemented on a DSP platform. The proposed system includes a device for capturing finger-vein images, a method for ROI segmentation, and a novel method combining blanket dimension features and lacunarity features for recognition. The images from 600 fingers in the dataset were taken over long time interval (i.e., from summer to winter) by a prototype device we built. The experimental results showed that the EER of our method was 0.07%, significantly lower than those of other existing methods. Our system is suitable for application in mobile devices because of its relatively low computational complexity and low power consumption.

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Design and Implementation of Universal Data Converter

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ABSTRACT

A universal data converter is designed using PHILIPS 89V51RD2BN mic controller liquid crystal display (LCD), 8051 development board, etc. This system generates seven different number system codes for any given input data. The program for micro controller is developed in embedded C- language and is converted to HEX file using keil U vision2 cross compiler. This system can perform 56 conversions which are mostly used in industrial applications. The input number system and the output number system are selected among eight number systems by comparing these two 8-bit code word is generated .by using code word data is converted from the given number system to desired number system.

Key words

Liquid crystal display (LCD), PHILIPS 89V51RD2BN micro controller, 8051 development board, keil U vision2 cross compiler.

1. INTRODUCTION

A number system defines a set of values used to represent quality. Number system have prominent role in everyday life such as communication, business dealings, traffic control, space guidance, medical treatment, and internet, weather identification and many other commercial, industrial and enterprises.

Many number systems are in use in digital technology. The most common are the decimal, binary, octal and hexadecimal systems. Understanding these number systems is important because their use simplifies other complex topics including Boolean algebra and logic design, signed numeric representations and character code digital circuit s are inherently binary in nature.

In present calculators, we have octal, decimal, hexadecimal and binary conversions, which are used by students, but for scientific and communication purpose, we need more conversions. so we tried to develop a unique converter which converts the data from one form to other form covering almost all number systems used in industrial application.

Unlike general purpose scientific calculators where multiple key selection is required to shift between numbers system provides unique and simple key selection to generate desired output and thus making the system ease to use without much skills. This is particularly helpful for technicians working in industries.

In HTML, (as well as in CSS and other web languages) color code is in hexadecimal and is preceded by #, in the format # RRGGGBB. Gray code is designed to minimize errors during the transitions working in industries.

For display purpose each decimal digit is often represented by 4-bit binary number in a system called binary coded decimal (BCD).the octal (base-8) and hexadecimal (base-16) number systems are both used for same purpose to provides efficient means to representing the large binary system. Binary number system also helps in encryption, low level programming, and hardcore particles like hex editing. For every application like HTML browsers, jpg files, power point presentations and data link layers (DLLs) in computer networking.

2. DESCRIPTION OF NUMBER SYSTEM

Number systems, decimal, binary, octal, hexadecimal, gray, excess-3, BCD-8421, BCD-2421.

Overview

Decimal number system

In decimal number system we can express any decimal number in units, tens, hundreds, thousands and so on. For example the decimal number 5678.9 can be written as 5678.910 where the 10 is radix or base. It is very important because it is universally used to represent quantities outside a digital system.

Binary number system

Decimal number system with its ten digits is a base-ten system. Similarly, binary system consists two digits is also a base- ten system. The two binary digits (Bits) are 1 and 0.like digital system, in binary system each binary digit commonly known as bit, has its own value or weight. In binary system weight is expressed as a power of 2.

Octal number system

The octal number system uses first eight digits of decimal number system 0, 1,2,3,4,5,6,7.

Hexadecimal number system

The hexadecimal number system has a base 16 having 16 digits:0,1,2,3,4,5,6,7,8,9,A,B,C,D,E and F. it is another number system that is particularly useful for human communications with a computer. Although it is somewhat more difficult to interrupt than the octal number system, as it has become the most popular. Since base is a power of $2(2^4)$, it is easy to convert hexadecimal numbers to binary and vice versa.

Gray code

Gray code is special case of unit-distance code. In unit-distance code, bit patterns for two consecutive numbers differ in only one bit position. These codes are also called cyclic codes. Gray code are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV system and also used in labeling the axes of karnaugh maps.

BCD-8421

BCD is an abbreviation for binary-codded-decimal.BCD is a numeric code in which each digit of a decimal number is represented by a separate group of bits. The most common BCD code is 8421 BCD, in which each decimal digit is represented by a 4-bit binary number. It is called 8421 BCD because the weight associated with 4-bit are 8421 from left to right. This means that, bit 2 has weight 4, bit 1 has weight 2 and bit 0 has weight 1.

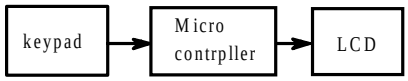
BCD-2421

The 2421 BCD is another self complementing code. Unlike excess-3, it has the additional feature that its 4-bit code groups are weighted. Since two positions have the same weight, there are two possible bits patterns that could be used to represent some decimal digits, but only one of those patterns is actually assigned.

Excess-3 code

Excess-3 code is a modified form of a BCD numbers. The excess-3 code can be derived from the natural BCD code by adding 3 to each code number. For example, decimal 12 can be represented in BCD as 0001 0010. Now adding 3 to each digit we get excess 3 codes as 0100 0101(12 in decimal).

3. BLOCK DIAGRA



Through keypad selecting the input number system to the output number system. Keypad is connected to microcontroller.

3.1 Conversion table

The program is dumped in micro controller.Here the microcontroller is P89V51RD2BN.The output is displayed on LCD.

	Decimal	Binary	Hexa Decimal	Octal	Gray Code	EXCESS-3	BCD 8421	BCD2421
decimal	N V	1	2	3	4	5	6	7
Binary	8	NV	9	10	11	12	13	14
Hex decimal	15	16	NV	17	18	19	20	21
Octal	22	23	24	NV	25	26	27	28
Gray code	29	30	31	32	NV	33	34	35
Excess-3	36	37	38	39	40	NV	41	42
BCD 8421	43	44	45	46	47	48	NV	49
BCD 2421	50	51	52	53	54	55	56	NV

3.2 Table: *OUTPUT NUMBER SYSTEM*

DECIMAL	Binary	Octal	Hex decimal	Gray code	Excess-3	BCD 8421	BCD2421
0	0000	0	0	0000	0011	0000	0000
1	0001	1	1	0001	0100	0001	0001
2	0010	2	2	0011	0101	0010	0010
3	0011	3	3	0010	0110	0011	0011
4	0100	4	4	0110	0111	0100	0100
5	0101	5	5	0111	1000	0101	0101
6	0110	6	6	0101	1001	0110	1100
7	0111	7	7	0100	1010	0111	1101
8	1000	10	8	1100	1011	1000	1110
9	1001	11	9	1101	1100	1001	1111
10	1010	12	A	1111	NV	NV	NV
11	1011	13	B	1110	NV	NV	NV
12	1100	14	C	1010	NV	NV	NV
13	1101	15	D	1011	NV	NV	NV
14	1110	16	E	1001	NV	NV	NV
15	1111	17	F	1000	NV	NV	NV

4. Applications

Communication-to facilitate error correction in digital communication such as digital terrestrial television and some cable TV system, it can be used.

It finds its application in industry, research and development, education laboratory

Internet- in different web languages such as HTML and CSS, to develop any application it can be used.

Whether identification, and many other business related (money counting, message display), in small and large industries and enterprises.

5. Requirement Specification

Hardware Required

Power supply 5-volts, pc, keil cross complier, RS-232 serial cable, jumper and wires.

6. Conclusion & Future scope

Micro controller based universal data converter is constructed using easily available components and is very useful tool for code conversion, error detection in data transmission and many more applications. It finds its application in industry, research and development, education and laboratories etc. The designed system is very handy, cost effective, and reliable and very is to use for quick conversion .therefore enthusiasts researches and students can use this system.

By using this micro controller based universal code converter we can get 56 conversions it can be further enhanced by adding more conversions which are very useful in research and development purpose.

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Heart Rate Variability Analysis Methods

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ABSTRACT

Heart Rate Variability (HRV) is a non-invasive tool which can be used for stu of many physiological features of human body. Basically heart rate variability is a non stationary signal whose variation may contain indication of current disease or even imminent cardiac diseases. These indications may be present for whole day or may be present during certain times of day. Thus it is very strenous to analyze the data whole day and pinpoint or pick out the abnormality out of such huge amount of data. HRV can be analysed in time, frequency and non-linear domain.

Keywords

Heart rate variability, Time domain and Frequency domain analysis, Autonomic nervous system

I. INTRODUCTION

Heart rate variability (HRV) is a heart rate fluctuations about mean heart rate and is useful in investigating sympathetic and parasympathetic functions of autonomic nervous system and thus it tells risk of sudden cardiac death. Thus HRV is ability to access overall cardiac health and state of autonomic nervous system. HRV is a reliable reflection of the many physiological factors modulating the normal rhythm of the heart. It provide a powerful means of observing the interplay between the sympathetic and parasympathetic nervous systems. It shows that the structure generating the signal is not only simply linear, but also involves nonlinear contributions. Heart rate (HR) is a non stationary signal; its variation may contain indications of current disease, or warnings about impending cardiac diseases. The indications may be present at all times or may occur at random during certain intervals of the day. It is strenuous and time consuming to study and pinpoint abnormalities in huge data collected over several hours. Hence, HR variation analysis (instantaneous HR against time axis) has become a popular noninvasive tool for assessing the activities of the autonomic nervous system. Computer based analytical tools for in-depth study of data over daylong intervals can be very useful in diagnostics. Therefore, the HRV signal parameters, extracted and analyzed using computers, are highly useful in diagnostics.

II. INTERPRETATION OF ECG

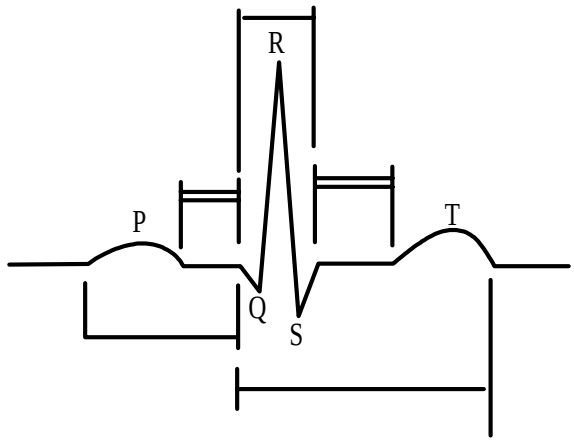

Figure 1 : *Typical ECG signal (Adapted from [6])*

P wave represents depolarization of atrial musculature. Horizontal segment preceding P wave is designated as baseline or isopotential line. QRS complex is the combined result of repolarisation of atria and depolarization of ventricles which occurs almost simultaneously. T wave represents ventricular repolarization whereas U wave (if present) is believed to be result of after potentials in ventricular muscle. P-Q interval represent time during which excitation wave is delayed in Purkinje fibers near AV node. Shape and polarity of each of these features vary with location of measuring electrodes and cardiologist take readings at several locations.

Working of heart

Our heart is made up of 4 chambers. The two upper chambers are called the left and right atria or auricles, while the lower two chambers are called the left and right ventricles. The atria are attached to the ventricles by fibrous, non-conductive tissue that keeps the ventricles electrically isolated from the atria. The right atrium and the right ventricle together form a pump to the circulate blood to the lungs. Blood brings needed nutrients and oxygen to tissue, and carries away metabolic waste and carbon dioxide for excretion through the kidneys and the lungs, respectively. Oxygen-poor blood is received through large veins called the superior and inferior vena cava and flows into the right atrium. The right atrium contracts and forces blood into the right ventricle. The right ventricle then pumps the blood to the lungs where the blood is oxygenated. Similarly, the left atrium and the left ventricle together form a pump to circulate oxygen-enriched blood received from the lungs via the pulmonary veins to the rest of the body. Pumping is performed with synchronised motion. The right and left atria contract together to force-fill the ventricles, and then the right and left ventricles contract together to forcefully pump blood to the lungs and other parts of the body, respectively. The time duration during which the ventricles contract is known as "systole" while the time duration during which the ventricles relax to receive blood is called "diastole". The left ventricle typically has a muscular wall about three times as thick as that of the right ventricle because it has heavier workload to circulate blood to the rest of the body. The muscle wall of the heart is made up of three layers. The inner layer, called the endocardium, lines the chambers of the heart. The centre layer is the myocardium, which forms the bulk and provides the contractile force for pumping. This layer of myocardium is further divided into the subendocardial area which is the inner half of the myocardium, and the subepicardial area, the outer half. The outermost layer of the heart wall overlying the myocardium is called the epicardium. The entire heart is encased in a thin membrane called the serous pericardium, which is made up of 2 layers viz the visceral (inner) and parietal (outer) pericardium. Pericardial fluid between these 2 layers minimizes friction against heart movements as the heart beats. Action potential in heart originates near top of right atrium called pacemaker or sinoatrial (SA) node.

Autonomic nervous system

The ANS have sympathetic and parasympathetic components. Sympathetic stimulation, occurring in response to stress, exercise and heart disease, causes an increase in Heart Rate by increasing the firing rate of pacemaker cells in the heart's sino-atrial node. Parasympathetic activity, primarily resulting from the function of internal organs, trauma, allergic reactions and the inhalation of irritants, decreases the firing rate of pacemaker cells and the HR, providing a regulatory balance in physiological autonomic function. The separate rhythmic contributions from sympathetic and parasympathetic autonomic activity modulate the heart rate (RR) intervals of the QRS complex in the electrocardiogram (ECG), at distinct frequencies. Sympathetic activity is associated with the low frequency range (0.04–0.15 Hz) while parasympathetic activity is associated with the higher frequency range (0.15–0.4 Hz) of modulation frequencies of the HR. This difference in frequency ranges allows HRV analysis to separate sympathetic and parasympathetic contributions evident. This should enable preventive intervention at an early stage when it is most beneficial.

III. Techniques of analyzing HRV

Time domain analysis

Two types of HRV indices are distinguished in time domain analysis. Beat-to-beat or STV indices represent fast changes in heart rate. LTV indices are slower fluctuations (fewer than 6 per minute). Both of these indices are calculated from the RR intervals occurring in a chosen time window (usually between 0.5 and 5 min). From the original RR intervals, a number of parameters can be calculated such as SDNN, the standard deviation of the NN intervals, SENN is the standard error, or standard error of the mean, SDSD is the standard deviation of differences between adjacent NN intervals, RMSSD, the root mean square successive difference of intervals, pNN50%, the number of successive difference of intervals which differ by more than 50 ms expressed as a percentage of the total number of ECG cycles analyzed. The statistical parameters SDNN, SENN, SDSD, RMSSD, NN50, and pNN50% can be used as time domain parameters. Geometrical methods present RR intervals in geometric patterns and various approaches have been used to derive measures of HRV from them. The triangular index is a measure, where the length of RR intervals serves as the x-axis of the plot and the number of each RR interval length serves as the y axis. The triangular interpolation of NN interval histogram (TINN) is the baseline width of the distribution measured as a base of a triangle, approximating the NN interval distribution (the minimum of HRV). This triangular index had a high correlation with the standard deviation of all RR intervals. But it is highly insensitive to artifacts and ectopic beats, because they are left outside the triangle. This reduces the need for preprocessing of the recorded data. The major advantage of geometric methods lies in

their relative insensitivity to the analytical quality of the series of NN intervals.

Frequency domain analysis

The time domain methods are computationally simple, but lack the ability to discriminate between sympathetic and para-sympathetic contributions of HRV. These studies of HRV employed the periodogram or fast Fourier transform (FFT) for power spectral density (PSD) estimation procedure consists of two steps. Given the data sequence $x(n\, 0 \le n \le N-1$, the parameters of the method are estimated. Then from these estimates, the PSD estimate is computed. But these methods suffer from spectral leakage effects due to windowing. The spectral leakage leads to masking of weak signal that are present in the data. The parametric (model based) power spectrum estimation methods avoid the problem of leakage and provide better frequency resolution than nonparametric or classical method. AR method can be used for the analysis of frequency domain. In AR method, the estimation of AR parameters can be done easily by solving linear equations. In AR method, data can be modeled as output of a causal, all pole, discrete filter whose input is white noise. The advantage of FFT based methods is the simplicity of implementation, while the AR spectrum yields improved resolution especially for short samples. Another property of AR spectrum that has made it popular in HRV analysis is that it can be factorized into separate spectral components. The disadvantages of the AR spectrum are the complexity of model order selection and the contingency of negative components in the spectral factorization. Nevertheless, it may be advantageous to calculate the spectrum with both methods to have comparable results.

Non-linear methods

Recent developments in the theory of nonlinear dynamics have paved the way for analyzing signals generated from nonlinear living systems. It is now generally recognized that these nonlinear techniques are able to describe the processes generated by biological systems in a more effective way. The technique has been extended here to study of various cardiac arrhythmias. The parameters like correlation dimension (CD), largest Lyapunov exponent (LLE), SD1/SD2 of Poincare plot, Approximate Entropy (ApEn), Hurst exponent, fractal dimension, a slope of Detrended Fluctuation Analysis(DFA) and recurrence plots.

Poincaré plot

Poincaré HRV plot is a graph in which each RR interval is plotted against next RR Interval. Thus it is a type of delay map. It is also known as Scatter plot, scattergram Return map, phase delay map and Lorenz plot. Poincaré plot is a valuable HRV analysis technique due to its ability to display nonlinear aspects of the interval sequence. Poincaré plot analysis is an emerging quantitative-visual technique whereby the shape of the plot is categorized into functional classes that indicate the degree of heart failure in a subject. The plot provides summary information as well as detailed beat-to-beat information on the behavior of the heart. Cardiac systems are nonlinear in their function due to which support is increasing for nonlinear analysis techniques and quantitative descriptors. Due to all this Poincaré plot is becoming a popular technique due to its simple visual interpretation and its proven clinical ability as a predictor of disease and cardiac dysfunction.

Recurrence plot

Recurrence plot (RP) is a graph which shows all those times at which a state of the dynamical system recurs. In other words, the RP for a given moment in time reveals all the times when the phase space trajectory visits roughly the same area in the phase space. The knowledge of transitions between regular, laminar or chaotic behavior is essential to understand the underlying mechanisms behind complex systems. While several linear approaches are often insufficient to describe such processes, there are several nonlinear methods which however require rather long time observations. To overcome these difficulties, we propose measures of complexity based on vertical structures in recurrence plots and apply them to heart rate variability data. Applying these measures to heart rate variability data, we are able to detect and quantify the laminar phases before a life-threatening cardiac arrhythmia occurs thereby facilitating a prediction of such an event. However, observational data of these systems are typically rather short. Linear methods of time series analysis are often not sufficient and most of the nonlinear techniques such as fractal dimensions or Lyapunov exponents have drawback of dimensionality and require rather long data series. To overcome these difficulties other measures of complexity based on the method of recurrence plots (RP) are used.

Detrended fluctuation analysis

Detrended fluctuation analysis (DFA) measures the correlation within the signal. The correlation is extracted for different time scales as follows. First, the RR interval time series is integrated where RR is the average RR interval. Next, the integrated series is divided into segments of equal length n. Within each segment, a least squares line is fitted into the data. Let yn(k) denote these regression lines. This computation is repeated over different segment lengths to yield the index F(n) as a function of segment

length n. Typically F(n) increases with segment length. A linear relationship on a double log graph indicates presence of fractal scaling and the fluctuations can be characterized by scaling exponent (the slope of the regression line relating log F(n) to log n).

Different values indicate the following

$\alpha = 1.5$: Brown noise (integral of white noise)

$1 < \alpha < 1.5$: Different kinds of noise

$\alpha = 1$: 1/f noise

$0.5 < \alpha < 1$: Large values are likely to be followed by large value and vice versa

$\alpha = 0.5$: white noise

$0 < \alpha < 0.5$: Large value is likely to be followed by small value and vice versa

Typically, in DFA the correlations are divided into short-term and long-term fluctuations.

IV. CONCLUSION

Heart rate variability analysis has become an important tool in cardiology, because its measurements are noninvasive and easy to perform, have relatively good reproducibility and provide prognostic information on patients with heart disease. HRV has proved to be a valuable tool to investigate the sympathetic and parasympathetic function of the ANS, especially in diabetic and post-infarction patients. Spectral analysis of HR has clarified the nature of diabetic autonomic neuropathy and of other neurologic disorders that encounter the ANS. Nonlinear parameters can be used to analyze the health of the subjects. In the future, individual therapy adjustments to aim at the most favorable sympathetic-parasympathetic balance in post-infarction patients might be possible with the help of HRV analysis.

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Design and Development of Embedded based pH Measurement System for Soil Analysis

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ABSTRACT

The objective of this paper is to design and development of Embedded based system for pH measurement in soil samples. Almost all processes containing water have a need for pH measurement [1]. To attain high crop yields, farmers must condition their fields to the correct pH value. Soils can be naturally acidic or alkaline and this can be measured by testing the pH value of the soil. Having the correct pH is very important for healthy plant growth. Hence, it is important to understand more about soil pH, and to be aware of the long-term effects of different soil management practices on soil pH [18-19]. In this present work done the data acquisition system is implemented by using pH-ion selective electrode as a sensing device, signal-conditioning circuit, digitization unit, processing unit with a Rabbit Core Module (RCM). The measured output can be monitored in dual manner: stand-alone system and web based monitoring.

Keywords

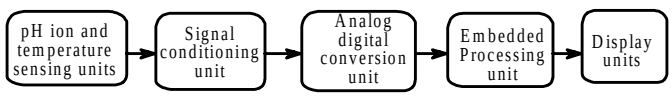
Soil pH, Ion Selective Electrode (ISE), data acquisition system, Rabbit Core Module (RCM)

I. INTRODUCTION

Soil pH influences many facets of crop production and soil chemistry, including availabilities of nutrients and toxic substances, activities and nature of microbial populations, and activities of certain pesticides. Soil pH is defined as the negative logarithm (base 10) of the H+ activity (moles per liter) in the soil solution [6-7]. As the activity of H+ in the soil solution increases, the soil pH value decreases. Soils with pH values below pH 7 are referred to as “acidic” and those with pH values above pH 7 as “alkaline”; soils at pH 7 are referred to as “neutral” [8]. Thus, a change in soil pH due to the addition of an acid or base is usually much less than predicted by neutralization based only on the quantity of acid or base present in the soil solution (as given by the soil pH). Lime requirement tests for soils, which generate recommendations for effecting relatively long-term changes in soil pH, are designed to evaluate the buffering power of soils [12-15].

In the present study, an embedded based system for pH measurement system is designed and constructed. It works on the principle of an electrochemical cell [16], which consists of a pH ion selective electrode as the working electrode, through which percentage of hydrogen concentration is to be estimated. The cell produces an emf proportional to the concentration of the hydrogen ion [17]. The emf produced is of the order of a few millivolts and it is generally of the order of 59.16 millivolts/decade [8]. The potential of the pH ion selective electrode slightly depends on the temperature of the solution also, which is to be compensated [18]. The emf generated in the electrochemical cell is given to a high input impedance amplifier [19]. The output of the amplifier, which is in analog form, is converted in to digital form with the help of analog to digital converter [20]. An embedded processing unit [21] is used to acquire process and display the results corresponding to pH concentration with appropriate interfacing devices [22]. The necessary software to operate the system is developed in Dynamic C language [23]. In the system, the result is displayed in two ways- one is on LCD and the second one is on the web page at both local and remote systems. The web page design is based on Hyper Text Markup Language [25-26]. To provide online communication, Apache web server software [24] is also used in the local system with internet connection.

II. Hardware implementation



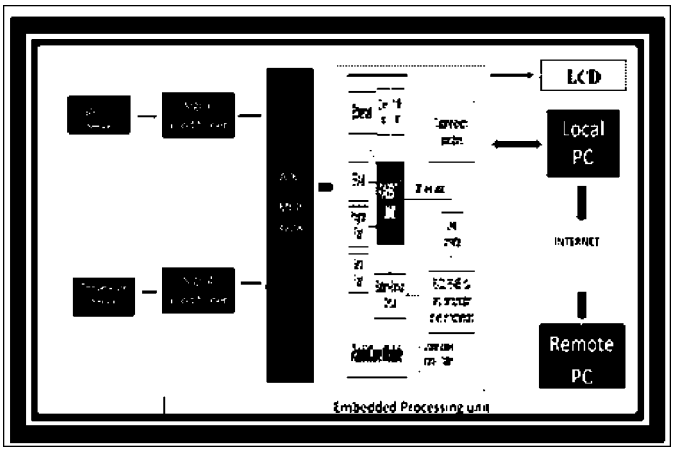


Fig.1: *Block diagram of embedded based system for the measurement of pH*

The block diagram of embedded based system for the measurement of pH is shown in Fig.1. The system consists of following functional units.

1. pH ion sensing unit
2. Temperature sensing unit
3. Signal conditioning unit
4. Analog to digital conversion unit
5. Embedded processing unit and
6. Display units

1. pH ion sensing unit

pH ion sensing unit is an electrochemical cell consists of pH ion selective electrode as the working electrode, and a reference electrode both are immersed in an aqueous solution whose ion concentration is to be estimated [18] and is shown in Fig.2. The electrochemical circuit [27] is completed by connecting the electrodes to a sensitive milli-volt meter using special low-noise cables and connectors. A potential difference is developed across the ISE membrane when the target ions diffuse through, high concentration side to the lower concentration side [19].

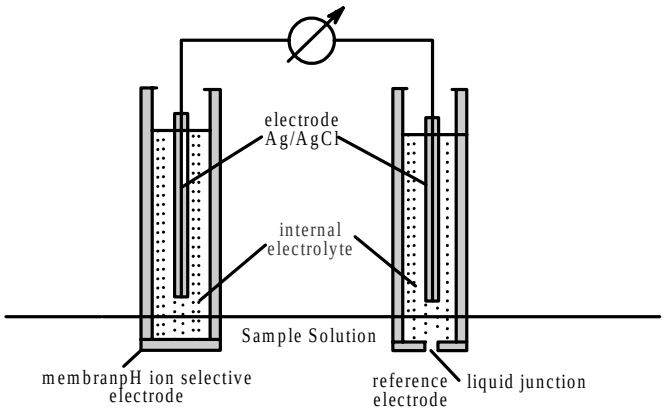


Fig .2: *pH Electrochemical Cell*

pH ion selective electrode

A pH sensor is a device, which converts the pH value in to corresponding voltage when immersed in a solution. The pH sensor used in the present study is a combination of electrodes, which combines both the working (glass) electrode and reference electrode into one body.

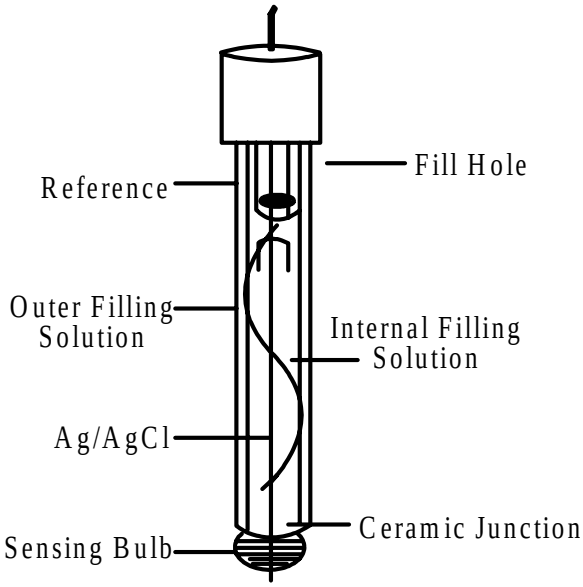


Fig.3 : *Internal structure of pH electrode*

The internal structure of pH electrode is shown in Fig.3. Most natural waterfalls are in the range of 5-8. It gives 2 Volts for pure water sample [3].The bottom of a pH sensor balloons out into a round thin glass bulb. The pH sensor is best thought of as a tube within a tube. The inner most tube contains an unchangeable saturated KCL and a 0.1 M HCL solution, acting as the cathode terminal of the reference electrode [1-2]. The anodic terminal wraps itself around the outside of the inner tube and ends with the same sort of reference electrode as was on the inside of the inner tube. The pH ion sensitive electrode used in the present study is shown in Fig.4.

Fig.4 : *pH ion selective electrode*

2. Temperature sensing unit

The pH sensor is temperature dependent parameter. Hence, the temperature of the liquid is measured and pH is compensated with temperature. Therefore, temperature

sensing unit is added with the pH measurement system. In the present study, precalibrated temperature sensor LM35 is used. It gives direct centigrade-scaled output voltage. It varies linearly with respect to temperature. For every degree rise in temperature, there is a corresponding change of 10mV at the output voltage of the sensor. Therefore, no signal conditioning is required for temperature measurement before ADC reading.

3. Signal conditioning unit

The pH ISE, sense the liquid hydrogen concentration and it converts its equivalent electrical signal, which is in very low magnitude voltage range, typically of the order of milli-volts range. To interface this low magnitude voltage with the ADC, little amplification is essential. It is done through very high input impedance JFET operational amplifier TL081 is used in signal conditioning circuit and is shown in Fig.5. The output of the pH sensing unit is connected to the non-inverting input terminal (pin no: 3) of the opamp and ground.

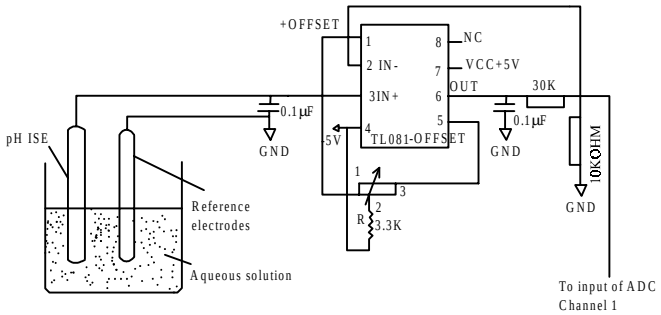


FIG.5 : *Signal Conditioning Circuit*

The signal is amplified with the gain of 4 (as per the circuit configuration shown in Fig.5).

Vout = Av * Vi

Av = [1 + Rf / Ri] = [1 + 30 K / 10 K] = 4. Where,

Vout = Output voltage of signal conditioning circuit,

Av = Voltage gain of non-inverting mode operational amplifier,

Rf = Feedback resistor $(30\,K\Omega)$, and

Ri = Input resistor $(10\,K\Omega)$.

The offset voltage is adjusted through variable resistor (POT) connected between pin no: 4 and 5. The output is taken at the pin no : 6. This amplified output is directly connected to one of the 8-channels of ADC.

After signal conditioning process, the amplified output of pH sensing unit and temperature sensor output are connected to the 1st and 3rd channels of ADC MCP3208 as shown in Fig.6. The ADC is an eight channel, 12 bit, serial ADC. The other six channels are for other measurement purposes.

The interfacing of ADC and LCD with the embedded processing unit is also presented in schematic diagram of an embedded based system for pH measurement as shown in Fig.6.

The schematic diagram is developed by using the Express-SCH software. The entire circuit is developed on general purpose PCB. The entire circuitry is placed in an iron box of 2mm thick. The dimensions of the box are- height : 3.5 inches, width : 10.1 inches and length is 12.2 inches respectively.

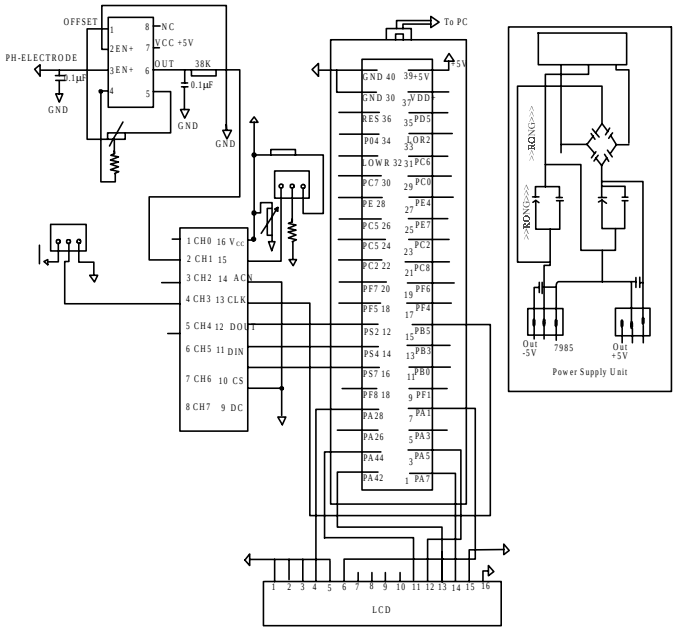


Fig. 6 : *Schematic Diagram of pH Measurement System*

III. SOFTWARE IMPLEMENTATION

The main role of the software in the present study is to govern the following activities.

1. To provide conversion of analog form of pH and temperature values in to digital form so that the embedded processor can process the data.
2. To measure the temperature of any solution with an accuracy of + 0.1^0 C.
3. To calibrate the pH ion sensitive electrode using standard solutions by means of software to find the slope of the pH ion sensitive electrode and to store the slope value.
4. To make the different functional units of the system work in a systematic and sequential manner.
5. To compute, transmit and display of pH ion

concentration and temperature values.

6. To provide display in two ways- one is on LCD of the instrument and the other is on webpage at local and remote PCs via intra and inter nets.
7. To provide the web based data acquisition system through internet by configuring the embedded based system for pH measurement system.

The flow chart diagram for the measurement of pH ion measurement is shown in Fig.7. The necessary software in the present study are developed in Dynamic C language and HTML to implement these tasks for effective functioning of the system.

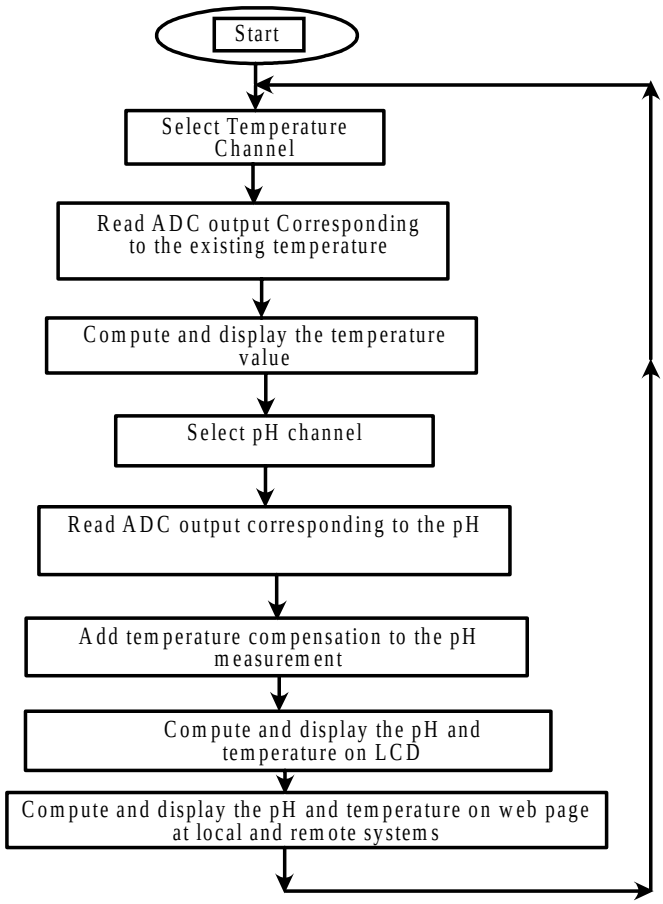


Fig.7 : *Flow chart diagram of pH measurement system*

IV. CALIBRATION OF THE SYSTEM

1. For calibration, get ready 3 standard buffer solutions of pH values 4, 7, and 9.18.
2. Rinse the pH electrode with distilled water thoroughly and bolt it dry with a soft tissue paper before immerses the electrode in the buffer solutions every time.
3. First, dip the electrode in pH 7 standard buffer solution and keep it in the solution until the reading is stable. Then the voltage at the channel-1 (pH is measured at CH-1 of ADC) is noted.
4. Then, dip the electrode in pH 4 standard buffer solution and keep it in the solution until the reading is stable and the voltage at the CH-1 is noted.
5. Finally, dip the electrode in pH 9.18 standard buffer solution and keep it in the solution until the reading is stable and the voltage at the CH-1 is noted.
6. By using these three different voltages at three solutions, slope of the electrode is calculated and is approximately 59 MV/decade.

The pH electrode characteristics are shown in Fig.8. By using the embedded based system for pH measurement at three buffer solutions is shown in the Table.1. The same buffer solutions readings are compared with the voltages obtained from the existing pH meter of Elico make. The values of the present study are in good agreement with these values. The system measures the pH values with a precision of ± 0.01. The measurement is observed on LCD and on web page via internet. The LCD results are shown in Fig.9. The web page results when pH electrode is dipped in buffer solutions 4, 7 and 9.18 are shown in Figures 10.a,b and c respectively.

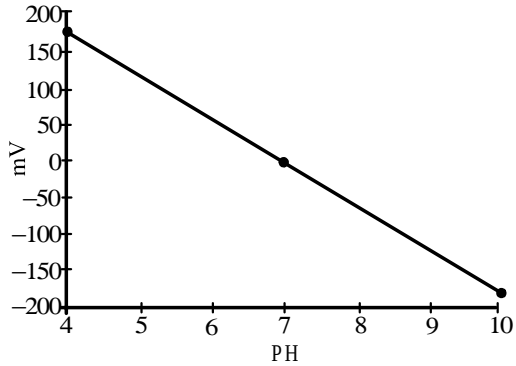


Fig.8 : *Output characteristics of pH ion selective electrode*

Table.1: *pH measurement of standard solutions*

S.N0:	Standard Buffer Solutions	Measurement values in the present study	Measurement Values of the existing Ph meter of Elico make
1	4.0	4.0	4.02
2	7.0	7.0	7.10
3	9.18	9.18	9.20

FIG.10.a: *pH value displayed on web-page when pH electrode is dipped in the pH-4 buffer.*

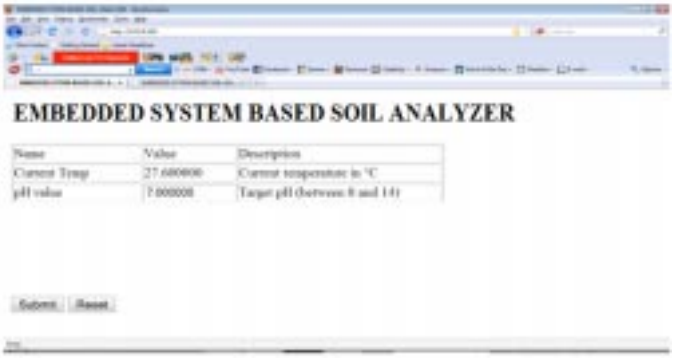


FIG. 10.b : *Web page result of pH and Temperature, when pH electrode is dipped in the pH-7 buffer solution.*

FIG.10.c : *Web page result of pH and Temperature, when pH electrode is dipped in the pH-9.18 buffer solution.*

V. MEASUREMENT OF pH IN SOIL SAMPLES

Measurement Procedure

1. Take the soil sample and add distilled water with 1:2 ratio.
2. Stir the solution for a particular period and dip the sensor in the sample solution.
3. Read the temperature in the soil sample and in the atmosphere.
4. As pH is temperature dependent, it varies with respect to temperature. Hence, the temperature compensated pH measurement is included.

Precautions

- Clean the electrode with double distilled water and blot them dry for every time before and after the test.
- The pH electrode is kept in a pH 4.0 buffer solution when it is not used under test.

VI. RESULTS OF STAND ALONE SYSTEM

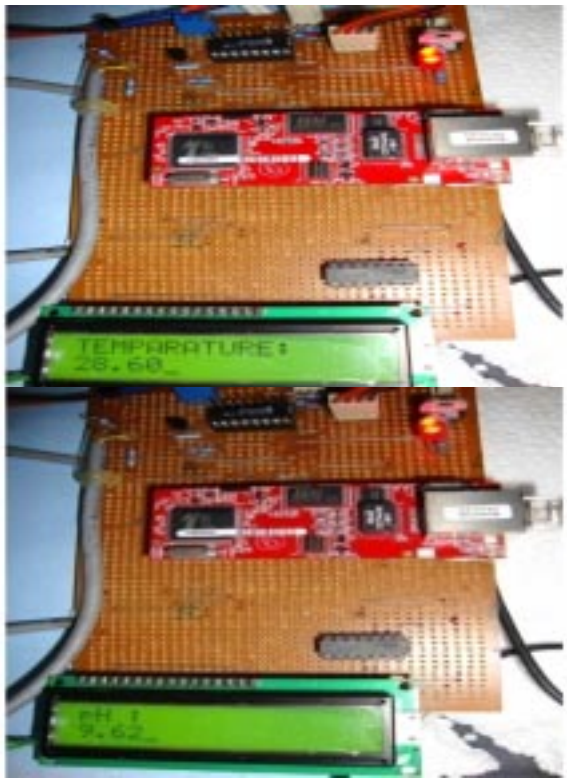


Fig.9 a, b : *The display of temperature and pH on LCD*

Soils can be naturally acid or alkaline, and this can be measured by testing the pH value of the soil. Having the correct pH is very important for healthy plant growth, so it is important to understand more about soil pH, and to be aware of the long-term effects of different soil management practices on soil pH. An embedded system based soil analyzer designed in the present study is used for the measurement of the pH in certain soil samples to test the validity and usefulness of the system. Before starting of the pH measurement in soil samples, the electrode of the system is to be calibrated. After calibration of the system, it can be used to measure the pH level in soil sample under test.

Table .2: *pH measurements in different villages in Anantapur district*

S.No.	Village	Mandal	pH Measurement in present study	pH Measurement @ Soil testing office, Anantapur
1	Y.Kothapalli	Atmakur	6.66	6.65
2	Garudapuram	Kalyanadurg	7.35	7.36
3	Mallapuram	Kalyanadurg	6.13	6.17
4	Mangam Palli	Settur	6.72	6.80
5	Gurave Palli	Kundurdi	7.56	7.58
6	Pesarakunta	Rapthadu	6.69	6.70
7	Mucharani	Dharmavaram	6.83	6.84
8	Kadadharakunta	Kuderu	6.65	6.64

VII. CONCLUSION

In the present study, soil samples are collected from different places in Anantapur district and their pH is measured with an embedded system based soil analyzer. The measurements are shown in Table 2. The same soil samples are tested with the equipment of soil testing office in Anantapur. These results are also presented in the same Table for comparison purpose. On observation of these two readings, the present study measurements are in good agreement with the soil testing office readings. In the present study, all the tested values are within the pH range of 6.13-7.56. As per the literature analysis [22-24], the pH range 6.5-7.5 is practically neutral and this is the best range for most of the crops. In the present study, Mallapuram soil is slightly acidic and the rest of the soils are within the optimum range.

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